NexGen Vertical GaN™ Power Devices

Superior Figure of Merit (FoM) for Hard and Soft Switching Applications
Content

• Types of Operations for Power Converters
  – Hard Switching Operation
  – Soft Switching Operation

• Device Figures of Merit (FoM) for Power Converters
  – Hard Switching Operation
  – Soft Switching Operation

• Comparison of various Power Devices and their FoMs
NexGen Vertical GaN™ eJFET: Simple GaN-on-GaN 3D Structure

100+ patents on proprietary design of eJFET, drift layer growth and manufacturing process

1. Basic Function of a Switch
   - Gate action causes switching
   - OFF: Gate closed, no current
   - ON: Gate open, current flow
   - Current flows from Drain to Source

2. How the FET is Created in our Fab
   - Processing steps to create FET in Syracuse Fab
   - Grow GaN Drift Layer in Syracuse Fab
   - Buy GaN wafer

3. 3D Roadmap
   - Increased area for increased current
   - Thicker growth for higher voltage
   - Uses all three dimensions to create product roadmap

eJFET = enhancement mode junction field effect transistor
Power Devices are Operated in one of two modes:

- **Hard Switching**
  - Turn-on or turn-off transistor at any time – no regard to voltage or current across device
  - Applications – Solar String inverters, <75W power supplies, Motor drives
  - Key performance indicators (Figures of Merit) from datasheet parameters
    - Low Output Capacitance - $C_{oss}$
    - Low Charge from Gate to Drain - $Q_{gd}$

- **Soft Switching**
  - Turn-on or turn-off transistor only at zero voltage or zero current across device
  - Applications – Solar micro-inverters, >75W power supplies, EV systems, Motor drives
  - Key performance indicators (Figures of Merit) from datasheet parameters
    - Low Output Capacitance - $C_{oss}$

In comparing industry standard Figure of Merit (FoM), NexGen’s Vertical GaN™ devices provide the best FoM for both soft and hard switching.
Figure of Merit

• A “Figure of Merit” (FoM) characterizes an important technology or design quality

• In this presentation FoM is used to compare alternative technologies w/r to a specific application performance

• Conflicting properties are often used to calculate a FoM
  This identifies the underlying features of a technology or design, e.g.
  • A desirable small $R_{DS(on)}$ requires a large transistor device area
  • A desirable small capacitance or electric charge usually requires a small device area

  $\rightarrow$ Small $R_{DS(on)}$ and small capacitances or charges are usually conflicting properties

  $\rightarrow$ FoMs which combine both properties provide insight into the intrinsic performance of a technology
Hard Switching Operation - Turn-on or Turn-off Switch Anytime

- Hard Switching occurs when, at the time the transistor channel opens or closes:
  - Voltage exists across the device
    - Losses due to nonrecoverable discharge of capacitances connected to drain ($C_{oss}$)
  - Current flows through the device while the voltage across the device is not negligible
    - Losses due to overlapping voltage across and current through the device
    - Transition speed from fully on to fully off or vice versa is important

- Applications
  - String Solar Inverters
  - <75W Adapters
  - Motor Drives
Transistor Turn-On-Transition

- The energy stored in a transistor output capacitance $C_{oss}$ is lost in each switching cycle when the transistor turns on.

  Stored energy = $\frac{1}{2} \times CV^2$

  Proportionality to $V^2$ makes it the most important loss mechanism in high voltage applications.

- Example ($C=100\,\text{pF}$):

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Stored Energy @ $F_{sw} = 1,\text{MHz}$</th>
<th>Power @ $F_{sw} = 1,\text{MHz}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>@50V</td>
<td>0.125 µJ</td>
<td>0.125W</td>
</tr>
<tr>
<td>@400V</td>
<td>8 µJ</td>
<td>8W</td>
</tr>
</tbody>
</table>

** $C_{oer}$ is the equivalent fixed capacitor value which holds the same energy as $C_{oss}$ while $V_{DS}$ rises from 0 to the operational $V_{DS}$.**
Figures of Merit in Hard Switching Operation (2)

**V\textsubscript{DS}/I\textsubscript{D} Overlap**

- Plays role in both Transistor Turn-on & Turn-off transitions
  
  a) \(V\textsubscript{DS}/I\textsubscript{D}\) overlap is mainly depending on the rate \((di/dt)\) with which a current can change and e.g. charge/discharge capacitors.
  
  External parasitic inductances limit \(di/dt\) and therefore voltage changes – this is design dependent and not a switching device property.

  b) Speed with which the channel opens or closes
    - Channel resistance switches from \(\infty\) to \(R\textsubscript{DS(on)}\)
    - Dependent on external gate driver config & Transistor charge \(Q\textsubscript{gd}\)

  \[
  \text{FoM} = R\textsubscript{DS(on)} \times Q\textsubscript{gd}
  \]
Soft Switching Operation - Turn-on or Turn-off Device at Zero Voltage or Current

- **Soft switching**
  - No Voltage across the device (ZVS)
  - No Current through the device (ZCS)
  - Or both

- **ZVS switching** is most important in high voltage applications
  - Eliminates the stored energy loss of $\frac{1}{2} * CV^2$ to zero because $V^2 = 0$

- **Resonant techniques** are generally employed to achieve ZVS or ZCS across a switching device

- **Applications**
  - >75W High Efficiency Power Supplies
  - Solar Micro-Inverters
  - DC-DC converters & on-board chargers for EV
  - Motor Drives
Loss Mechanisms in Soft Switching Operation

• Time related output capacitance $C_{o(tr)}^{**}$ is the most important parameter

• $C_{o(tr)}$ determines the dead time between turning off / turning on transistors in soft switching architectures, particularly in half or full bridge configurations
  – No energy is being transferred to the output during dead time
    $\rightarrow$ reduces application performance in higher switching frequency applications
  – The dead time can be reduced by increasing the current to discharge $C_{o(tr)}$ at the cost of additional resistive losses in the switching elements
    $\rightarrow$ reduces efficiency of power converters

**$C_{o(tr)}$ is the equivalent fixed capacitor value which would give the same charging time as $C_{oss}$ while $V_{DS}$ rises from 0 to the operational $V_{DS}$**
## Vertical GaN™ Comparison with Competitor Devices

<table>
<thead>
<tr>
<th></th>
<th>Si SJ MOSFET</th>
<th>SiC MOSFET</th>
<th>GaN eHEMT (Cascode)</th>
<th>GaN eHEMT</th>
<th>NXG2EA120P085 Vertical GaN™ eJFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV$_{DS}$</td>
<td>900</td>
<td>1200</td>
<td>900</td>
<td>650</td>
<td>1200</td>
</tr>
<tr>
<td>R$_{DS(on)}$ typ Tj=25°C</td>
<td>88</td>
<td>75</td>
<td>50</td>
<td>100</td>
<td>85</td>
</tr>
<tr>
<td>R$_{DS(on)}$ max Tjmax</td>
<td>248</td>
<td>124</td>
<td>132</td>
<td>335</td>
<td>195</td>
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<tr>
<td>Q$_G$</td>
<td>89</td>
<td>51</td>
<td>17.5</td>
<td>3.9</td>
<td>18.7</td>
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<tr>
<td>C$_{o(er)}$</td>
<td>159</td>
<td>65</td>
<td>160</td>
<td>47</td>
<td>12.4</td>
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<tr>
<td>C$_{o(tr)}$</td>
<td>429</td>
<td>80</td>
<td>274</td>
<td>75</td>
<td>14.4</td>
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<tr>
<td>Q$_{rr}$</td>
<td>29</td>
<td>0.22</td>
<td>0.164</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>HS FoM (R$<em>{DS(on)}$ * C$</em>{o(er)}$)</td>
<td>39.4</td>
<td>8</td>
<td>21</td>
<td>15.8</td>
<td>2.4</td>
</tr>
<tr>
<td>SS FoM (R$<em>{DS(on)}$ * C$</em>{o(tr)}$)</td>
<td>106</td>
<td>9.9</td>
<td>33</td>
<td>25.1</td>
<td>2.8</td>
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<td>Avalanche</td>
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<td>✓</td>
<td>✗</td>
<td>✗</td>
<td>✓</td>
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<tr>
<td>Package</td>
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<td>TO247-4</td>
<td>TOLL</td>
<td>Proprietary 5x6</td>
<td>DFN 8x8 TO247-4</td>
</tr>
</tbody>
</table>

### Outstanding Vertical GaN™ Features

- **Smallest Output Capacitances at comparable R$_{DS(on)}$ even with 1200V BV**
- **Best Soft Switching FoM enables very high Fsw**
- **Standard packages**
Summary

- FoM Metrics combine conflicting device properties to reveal the underlying technology performance

- FoM for Hard and Soft Switching operation Modes have been introduced

- In switch mode power supplies, the output capacitance of a switching device is of outmost importance
  - Determines directly switching losses in hard switching applications
    → limits directly the useful maximum switching frequency
  - Determines the required dead time to achieve ZVS in soft switching applications
    → limits the amount of energy transfer, particularly at high switching frequencies

- Gate charge $Q_{gd}$ is of lesser importance in high voltage applications and its effect can be mitigated with appropriate driver circuitry

- NexGen’s Vertical GaN™ devices delivers best-in-class FoMs for hard and soft switching applications, thus allowing for unrivaled high switching frequencies and reducing the size of switch mode power applications