Avalanche Ruggedness of 600/650 V Lateral GaN HEMTs and 1200 V Vertical GaN Diodes

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Outline

• Introduction
  – Avalanche test: Unclamped Inductive Switching (UIS) test
  – Open question: Avalanche capability in GaN-based power devices

• Avalanche test of 600/650 V lateral HEMTs
  – UIS tests under different temperatures
  – Failure analysis

• Avalanche test of 1200 V vertical GaN PN diode
  – Device static characterization
  – UIS tests under different temperatures

• Summary & Future Work
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Unclamped Inductive Switching (UIS): Avalanche Test

• Device surge-energy ruggedness is desired in many power applications: electric vehicle, motor drives, etc.

• Surge-energy capability typically characterized by unclamped inductive switching (UIS) test.

  • DUT on, inductor charged by VDD
  • Inductor current reaches desired value, DUT off
  • Energy stores in L goes through off-state DUT

Si / SiC power MOSFETs:
Surge energy is dissipated by avalanching in DUT
The Avalanche Phenomenon

- **Impact ionization + positive feedback**
  Multiplied electron-hole pairs at junction

- **Built-in safety mechanism**
  Accommodate high current at $BV_{AVA}$
  Recoverable within certain energy $E_{AVA}$: Key metric for robustness

- **Breakdown voltage increases with temperature**
  (Evidence for avalanche mechanism in practice for GaN & 4H-SiC)

Key to avalanche: PN junction connected to electrodes
Lateral GaN v.s. Vertical GaN

- 2DEG: Induced by piezoelectric effect: no doping
- No PN junction connected to electrodes
- Commercialized from 15 V to 650 V (→ 900 V)

Open Questions

- How does GaN HEMT withstand/dissipate surge energy?
- What determines the withstand capability?
- What is the failure/degradation mechanism?
- Is there robust avalanche in GaN vertical PN diode?
- Is the avalanche energy comparable to Si / SiC MOSFETs?
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Single-event UIS Test: DUTs

**Company A:** Gate Injection Transistor (GIT)
Device rating: 600 V, 31 A

$V_{GS(\text{on})}$ is clamped at 3.0~3.4 V
(same as GaN PN diode $V_f$)

**Company B:** Schottky p-gate HEMT (SP-HEMT)
Device Rating: 650 V, 30 A.

$V_{GS(\text{on})}$ can safely go up to 7 V
Temperature Adjustable UIS Test Setup

Presented in PMC review, Dec. 2019

New board & setup enabling high-T tests

Mother Board: Power loops
Daughter Card: Gate Driving Loop + DUT

\[ V_{DD} = 30 \text{ V} \]
\[ V_{GS(ON)} = 5 \text{ V (clamped to 3.0\textasciitilde3.4 V on GIT)} \]
\[ V_{GS(OFF)} = -5 \text{ V} \]

A TO-220 power resistor was used to heat up the DUT

High temperature FR-4 was used for the PCB
UIS Test Result – Safe Withstanding

Withstanding process:

• I: Device on, inductor charging.

• II: Device turn-off.

• III: Resonance between inductor & device $C_{\text{oss}}$, little energy dissipation in this stage.

• IV: Device 3\textsuperscript{rd} quadrant conduction, resistive energy dissipation via device, inductor is discharged by the power supply.

GaN HEMTs withstand surge energy by LC resonance, with minimal resistive energy dissipation in the resonant withstand process

UIS Test Result – Failure Waveforms

Company A: GIT

- All terminals show short, gate control lost

Company B: SP-HEMT

- Gate is still functional after the failure

Gate is still functional after the failure

All terminals show short, gate control lost

V_m leads to device failure shows little dependence on surge voltage duration within tens of nanoseconds.

GaN HEMT surge energy capability is almost solely limited by overvoltage capability
High temperature UIS: Safe withstanding waveforms

Company A: GIT

L = 100 uH
Charging time = 8 μs

Charging time = 10 μs

Withstand waveform shows little dependence on temperature
GaN HEMTs $C_{oss}$ changes little with temperature

Company B: SP-HEMT

L = 100 uH
Charging time = 10 μs
High Temperature (175 °C) UIS: Failure Waveforms

DUTs failed at high temperature show same failure waveforms. It is believed the failure locations and mechanisms don’t change.
$V_m$ leads to failure see little change in high temperature UIS test. Failure in UIS test is not related to temperature and is a E-field induced failure.
Failure Analysis: GIT – I-V Characterization

Gate remains functional

Failure between drain & substrate

I_{DS} (A)

25
20
15
10
5
0

V_{GS} (V)

0
1
2
3
4
5

1.0 \times 10^{-3}

I (A)

0.0

-1.0 \times 10^{-3}

V (V)

-6
-4
-2
0
2
4
6
Failure Analysis & Mixed-mode Simulation: GIT

FIB (focused ion-beam) & TCAD simulation: Failure & Peak E-field @ drain
Failure Analysis & Mixed-mode Simulation: SP-HEMT

- Burning (in metal) & cracks (in GaN) found at drain.
- Cracks found at gate field plate but no failure shown in GaN layer in the gate region

TCAD Simulation: Peak E-field @ drain and floating gate field plate. Initial failure may locate at drain.
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Devices under Test

- **Vertical GaN PN diode**
  - 1.2 kV, > 100 A (pulsed)

- **Compare with commercial 1.2 kV SiC Devices:**
  - Merged PN Schottky (MPS) diode
  - Schottky barrier diode (SBD)
  - PN diode (i.e. body diode of MOSFET)

Epitaxy growth & device fabrication by NexGen Power Systems in NexGen’s 100-mm GaN-on-GaN facility in New York

<table>
<thead>
<tr>
<th>Properties</th>
<th>GaN-on-Si</th>
<th>GaN-on-GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lattice mismatch (%)</td>
<td>17</td>
<td>0</td>
</tr>
<tr>
<td>CTE * mismatch (%)</td>
<td>54</td>
<td>0</td>
</tr>
<tr>
<td>Dislocation density (cm²)</td>
<td>$10^8$-$10^9$</td>
<td>$10^3$-$10^6$</td>
</tr>
<tr>
<td>Max. epi-layer thickness (μm)</td>
<td>~5</td>
<td>≥40</td>
</tr>
<tr>
<td>Thermal resistance (°C·mm/W) [5]</td>
<td>~30</td>
<td>-4</td>
</tr>
</tbody>
</table>

*C: CTE: Coefficient of thermal expansion.


<table>
<thead>
<tr>
<th>Device Tech.</th>
<th>Vendor</th>
<th>Part #</th>
<th>Nominal Current @25 °C</th>
<th>Current @25 °C</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPS</td>
<td>Infineon</td>
<td>IDH05G120C5</td>
<td>5 A @161 °C</td>
<td>19.1 A</td>
<td>TO-220</td>
</tr>
<tr>
<td>SBD</td>
<td>Rohm</td>
<td>SCS205KG</td>
<td>5 A @150 °C</td>
<td>-</td>
<td>TO-220</td>
</tr>
<tr>
<td>PN</td>
<td>Cree</td>
<td>C2M0160120D</td>
<td>-</td>
<td>25 A</td>
<td>TO-247</td>
</tr>
</tbody>
</table>
Characterization: Forward I-V

- Loss @ nominal current level (20 A):
  - SiC SBD < SiC MPS < GaN PN ≈ SiC PN
- Loss @ surge current level (60 A):
  - GaN PN close to SiC PN & MPS, << SiC SBD

\[ V_F = 3.4 \, \text{V} \]
\[ R_{on,\text{diff}} = \sim 90 \, \text{mΩ} \]

- Forward characteristics of GaN PN varies little with temperature

DUT: GaN PN
Characterization: C-V

- No reverse recovery
- C & $Q_C$ & $E_C$:
  - GaN PN < SiC MPS < SiC SBD < SiC PN

<table>
<thead>
<tr>
<th>DUT</th>
<th>Capacitance stored energy ($\mu$J) ($V_R = 800$ V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN PN</td>
<td>4.89</td>
</tr>
<tr>
<td>SiC MPS</td>
<td>5.07</td>
</tr>
<tr>
<td>SiC SBD</td>
<td>7.36</td>
</tr>
<tr>
<td>SiC PN</td>
<td>20.21</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DUT</th>
<th>Total charge (nC) ($V_R = 800$ V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN PN</td>
<td>17.82</td>
</tr>
<tr>
<td>SiC MPS</td>
<td>18.40</td>
</tr>
<tr>
<td>SiC SBD</td>
<td>24.28</td>
</tr>
<tr>
<td>SiC PN</td>
<td>62.99</td>
</tr>
</tbody>
</table>

$Q_C = \int C(V) dV$

$E_C = \int_0^{V_R} C(V) V dV$
Characterization: Reverse I-V

- Breakdown voltage > 1200 V
- Leakage current @ 1200 V:
  \[ \text{GaN PN} \approx \text{SiC PN} < \text{SiC MPS} \approx \text{SiC SBD} \]
- Leakage increases with temperature
- BV increases with temperature
  \[ \rightarrow \text{Avalanche nature} \]
Unclamped inductive switching (UIS) circuit

- $S_1 = 1.7 \, \text{kV SiC MOSFET}$

**Test condition**

- 6 inductors: 920 nH to 81 mH
- 3 temperatures: 25 °C, 100 °C, 175 °C

**DUT: GaN PN**

$T = 25 \, ^\circ \text{C}$
$L = 920 \, \text{nH}$

- $BV_{AVA} = 1675 \, \text{V}$
- $I_{AVA} = 24.8 \, \text{A}$

Robust avalanche demonstrated
**UIS test**

- Robust avalanche capability under elevated temperatures

\[ L = 300 \, \text{uH} \]
\[ I_{D,\text{peak}} = 7.2 \, \text{A} \]

- Failure mode: Thermally induced destruction
  - Critical \( E_{AVA} \) roughly consistent with thermal conductivity:
    - GaN \((1.3 \sim 2) < 4H\text{-SiC} \,(3.7)\)

<table>
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<tr>
<th>DUT</th>
<th>Critical Ava. Energy (J/cm(^2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN PN</td>
<td>2.6</td>
</tr>
<tr>
<td>SiC MPS</td>
<td>5.0</td>
</tr>
<tr>
<td>SiC SBD</td>
<td>2.0</td>
</tr>
<tr>
<td>SiC PN</td>
<td>6.7</td>
</tr>
</tbody>
</table>

- **\( BV_{AVA} \)**: positive temp. coeff.
  - \( BV_{AVA} \) @ 175 °C
  - \( BV_{AVA} \) @ 100 °C
  - \( BV_{AVA} \) @ 25 °C

**Electric Breakdown field (MV/cm)**
**Thermal conductivity (W/cm-K)**
**Energy Gap (eV)**
**Saturated Electron Velocity \( \times 10^7 \, \text{cm/s} \)**
**Electron Mobility \( \times 10^5 \, \text{cm}^2/V\text{-s} \)**
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Summary – Avalanche Ruggedness of GaN Devices

➢ GaN HEMTs “avalanche capability” limited by transient breakdown voltage, the failure is induced by high E-field.
➢ Different failure locations were found in commercial GITs and SP-HEMTs
➢ Failure mechanisms, boundaries, and failure locations are not influenced by temperature.

Large-area 1.2 kV vertical GaN PN diodes with current up to 100 A, manufactured by NexGen
Vertical GaN-on-GaN PN diode demonstrated robust avalanche
Failure mode: thermally induced
GaN can avalanche!
Next Steps

• Repetitive UIS tests for lateral GaN HEMTs and vertical GaN PN diodes.
• Design and develop GaN HEMT surge ruggedness under converter mission profiles.
• Surge ruggedness of GaN transistors.

Thank you!

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