Driving NexGen's Vertical GaN eJFET with MOSFET Gate Drive ICs

Introduction

NexGen is advancing the performance of GaN transistors to a new level with a vertical enhancement mode JFET that eliminates many of the drive difficulties common to other lateral type GaN transistors. A significant advantage of NexGen's eJFET is the ease with which existing MOSFET gate drive ICs can be adapted to effectively drive the transistor.

Driving NexGen's GaN

Figure 1 shows a schematic representation of a simple network that interfaces a MOSFET gate drive IC with NexGen's GaN transistors. It uses a MOSFET gate drive IC with bias supply levels common to typical MOSFET applications. As seen in figure 2, the gate drive charges the input capacitance (C_{iss}=C_{gs}) to the miller plateau voltage (V_p) followed by discharging C_{gd}=C_{rss} from the peak drain voltage. The gate threshold voltage is 1.25V with channel current reaching over 30A at a 2.5V gate voltage. The gate to source diode conducts when the gate to source voltage exceeds the gate to source diode forward conduction voltage of roughly 3.5V. This leaves a narrow voltage range between when the device is fully on and when the gate diode begins to conduct. A low impedance drive interface, typical of an isolated gate MOSFET, would deliver excessive gate current above V_f. The interface network in figure 1 prevents this by including a capacitively coupled low impedance path in parallel with a current limited path between the gate driver IC and the GaN transistor. The Rt/Ct path delivers a high peak current for fast turn on and the Rd path limits the gate to source diode current to a safe level after C_t charges to the drive bias voltage minus the gate to source diode forward voltage level (V_{dd}-V_f). Another added benefit of the interface network is that the charge developed on C_t during the on time will also drive the gate voltage negative during the off time by V_{dd}-V_f below zero. This also provides immunity from false turn during a very fast drain voltage swing possible during hard switching turn off conditions.

Typical R_t values range from 1Ω to 20Ω and C_t will typically range from 1nF to 10nF. Nominal R_d values range from 500Ω to 2kΩ. R_d limits the gate diode forward current and will also discharge C_t during the off-time.

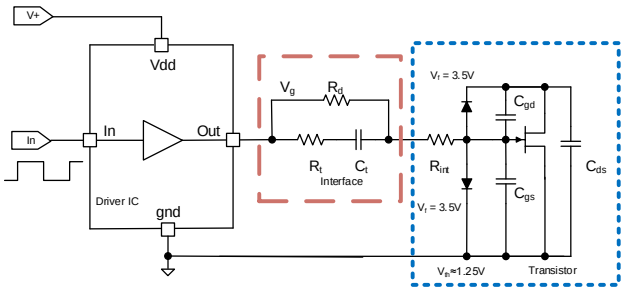

Figure 1. Interface for NexGen's e-mode Vertical GaN™ JFET. The blue short dashed box shows the JFET model and the large dashed red box shows the interface model. The standard driver is on the left.

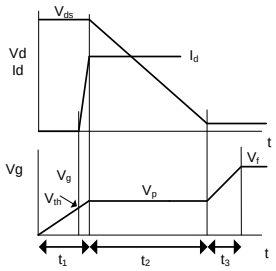

Figure 2. Turn-on Characteristics

Typical Gate Drive IC Characteristics

Table 1 lists just a few isolated and non-isolated 1MHz MOSFET gate drive ICs that can easily be adapted to drive NexGen GaN transistors. The isolated drivers are necessary for driving the transistors in a high voltage high side/low side totem pole configuration.

Parameter	Si8273	Si8238AD	UCC2751x	UCC21520	Unit
Maximum Driver side Supply Voltage	30	24	20	25	V
UVLO	3.5, 5.5, 8.3,12.2	5.8,8.6, 11.1,13.8	3.9	5.7,8.2	V
Isolation Output to Output	1.5	2.5	n/a	1.5	kV_{rms}
Isolation Input to Output	2.5	5	n/a	5.7	kV_{rms}
Output Current	1.8 source, 4.0 sink	2.0 source, 4.0 sink	4.0 source, 8.0 sink	4.0 source, 6.0 sink	A
Output Impedance	2.7 source, 1 sink	2.7 source, 1 sink	5 source, 0.375 sink	5.0 (1.47) source, 0.55 sink	Ω
Typical Rise/Fall Times	10.5/13.3 @ 200pF	12 @ 200pF	8 @ 1.8nF	6/7 @ 1.8nF	ns
Propagation delay matching			n/a	5	ns
Common mode transient immunity	200	45	n/a	100	V/ns

Table 1. Typical Driver Properties

Summary

The NexGen Vertical GaN™ JFET transistor gate drive interface must account for the characteristics of the transistor that differentiate it from the isolated Gate MOSFET. The transistor has a gate diode with a forward voltage of 3.5V, a very low threshold voltage 1.25V, and very fast switching speeds. A simple interface circuit allows the use of standard highspeed MOSFET gate drive ICs to meet these requirements.

The AC coupled / DC blocking interface network limits the current at the gate when the voltage exceeds the gate diode forward voltage. This network also forces a negative gate bias voltage during turn-off, thus making the transistor more immune to false turn-on due to the gate to drain capacitance coupling charge to the gate at turn-off. The interface network does this with a single bias rail common to isolated gate MOSFET drive applications.