NEXGEN POWER SYSTEMS

Vertical GaN™ Theory of Operation

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GaN enables advanced power electronic applications

Power switching devices have historically been built from silicon (Si). In recent years, it became apparent that the performance improvements necessary to deliver higher efficiency power conversion systems with increased power density and functional integration require substantially higher performance switching devices. Traditional Si super junction MOSFETs (Si-SJ) have reached their performance limits with respect to switching frequency and breakdown voltages while newer SiC devices, although allowing for a higher breakdown voltage (BV), are constrained to lower switching frequencies and are therefore limited in their ability to reduce the size of the power converters

Parameter	Si	SiC	GaN	
Bandgap, eV	1.12	3.26	3.45	Higher bandgap materials can operate at higher temperatures and withstand higher voltages **Best Material: GaN**
Critical Electric Field (E_c), MV/cm	0.3	2.2	3.3 – 3.7 (bulk GaN)	Higher dielectric breakdown translates into thinner, and therefore lower resistance, devices **Best Material: GaN**
Baliga Figure of Merit (FOM) $= \varepsilon_s \times \mu \times E_c^3$	1	675	3,000	Higher FOM means that devices are capable of operating at higher switching frequencies at higher voltages **Best Material: GaN**

Table 1 : GaN is the best material for power semiconductors

This leads to an increased interest in gallium nitride (GaN) which offers superior properties over Si and SiC with respect to increased breakdown voltage and high switching frequencies, thus enabling the substantial improvement of efficiency and power density needed by future power electronic applications.

NEXGEN POWER SYSTEMS™

Superior Device Properties of Vertical GaN™

Lateral GaN-on-Si Basic Device Construction and Key Properties

A range of GaN power devices have been introduced over the last several years.
Most of them are realized on hybrid substrate materials: relatively thin layers of GaN are grown on a Si or SiC substrate, thus creating GaN-on-Si or GaN-on-SiC devices.

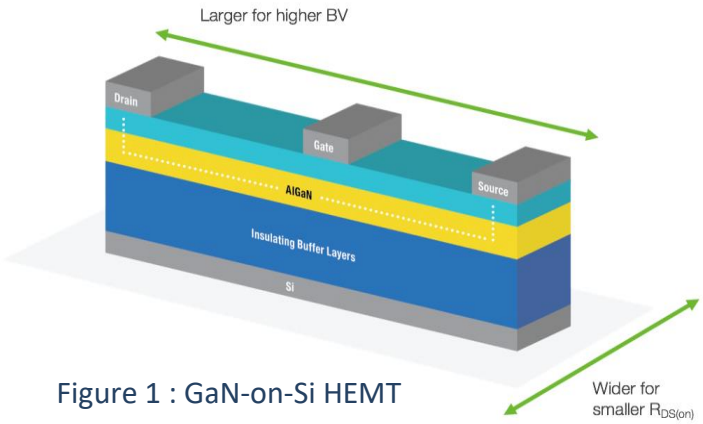


Figure 1 : GaN-on-Si HEMT

The discussion below focuses on GaN-on-Si but is similarly applicable to GaN-on-SiC.

Controlled by the gate-source voltage, the current between drain and source terminals flows in lateral direction in a very shallow layer of "2D Electron Gas" (2DEG) which is made of alluminium gallium nitride (AlGaN). Electron mobility is high and intrinsic capacitances are smaller than in Si-SJ and SiC devices, thus allowing for high switching speed.

However, the lateral device architecture has several inherent disadvantages:

- Heteroepitaxial device construction
  Lateral GaN-on-Si devices are built by epitaxially growing GaN layers on Si wafers, effectively combining materials with mismatched lattices and mismatched coefficients of thermal expansion (CTE). This requires the introduction of buffer layers to separate two materials with different lattice and thermal properties, but reliability weaknesses and performance compromises can still not be avoided

- Proximity of the drain-source channel to the device surface
  In a typical lateral GaN HEMT device, the channel is very close to the surface - on the order of 200 Å- making it susceptible to surface charges or charges in the near surface dielectrics. In addition, high fields are located near the surface with weaker material properties regarding critical electric fields compared to that in the bulk.
  The combination of bulk defects and near surface traps leads to the well-known phenomenon of dynamic $R_{DS(on)}$

- Breakdown Voltage (BV) Limitation
  The drain-source breakdown voltage of lateral GaN-on Si devices is primarily determined by the distance between drain and source. High breakdown voltages therefore require a large geometrical drain-source separation, resulting in a large $R_{DS(on)}$ which in turn requires a wider device to create practically useful $R_{DS(on)}$ values.
  Consequently, total device area, device capacitances and cost per device increase and limit lateral GaN-on-Si devices to approx. 600V breakdown voltage

- No Avalanche breakdown
  Avalanche breakdown is a key property of established Si and SiC devices and helps to protect applications under short term overvoltage conditions. Due to the absence of p-n junctions, lateral GaN-on-Si HEMTs do not avalanche. Instead, if the voltage stress is sufficiently high, the device eventually suffers a catastrophic breakdown. A large margin needs to be included above the rated breakdown voltage to ensure that the device is never subjected to the destructive breakdown. Even below the catastrophic breakdown, long term device reliability can be compromised when the device is repeatedly exposed for a longer time to voltages above the rated breakdown voltage.

- Thermal management
  Power switching devices generate heat during their switching and conduction cycle. This heat must be managed within a package or within a module in order to maximize the performance of the device. If the generated heat is not extracted from the device, $R_{DS(on)}$ has to be derated to ensure that the device does not encounter thermal runaway.
  The leadframe of a packaged device is the primary path to removing heat and usually the bottom/substrate of a device is attached to it.
  In lateral GaN, losses (heat) are generated near the top of the device and have to pass through material separating buffer layers and then through the Si base wafer. This is a suboptimal path compared with Vertical GaN™ where the heat is generated in the bulk of the material and passes through homogenous GaN to the substrate where the leadframe is attached
  Lateral devices can only be cooled efficiently only from one side of the device – the bottom. Vertical GaN™ devices can be cooled from the bottom and the top, enabling the performance to be maximized.

Vertical GaN™ Basic Device Construction and Key Properties

Historically, the use of Si or SiC substrates in hybrid GaN-on-Si(SiC) devices has been mainly motivated by perceived supply constraints and high cost of GaN substrates. This argument for hybrid devices is no longer sustainable: High quality GaN substrates with 4" diameter are available form a number of sources at competitive prices. Combined with the die size advantage of NexGen's Vertical GaN™ devices at a given breakdown voltage, cost equivalence of Vertical GaN™ with silicon is projected for 2022, enabling circuit and system designers to take advantage of the superior properties of Vertical GaN™ devices while supporting cost sensitive designs,

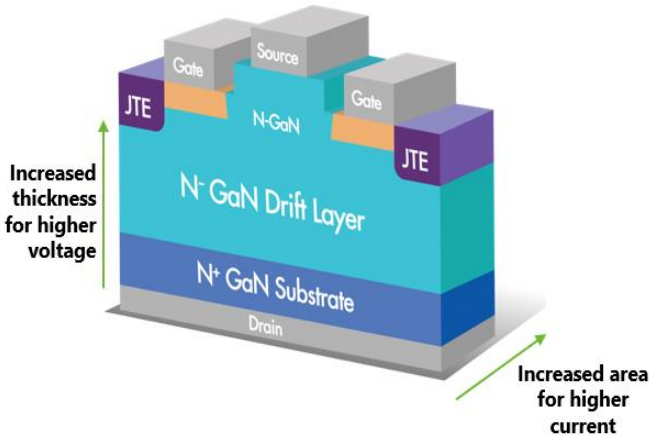


Figure 2 : Vertical GaN™ cross-section, conceptual view

NexGen's Vertical GaN™ transistors are formed by homoepitaxially growing thick GaN layers on a bulk GaN substrate (GaN-on-GaN). Lattice and thermal expansion mismatches as in heteroepitaxially grown GaN-on-Si layers do not exist. This allows very thick layers of GaN growth which enables the fabrication of devices with high breakdown voltage.
Vertical GaN™ transistors realize the full potential of the superior electron mobility and velocity as well as the high critical electrical field properties of GaN and overcome all limitations of lateral GaN-on-Si and more traditional Si-SJ and SiC devices:

- No Dynamic $R_{DS(on)}$
  Vertical GaN™ devices rely on current conduction through the channel and bulk drift layer. There is no 2DEG at surface interfaces to carry the drain-source current and hence no mechanism for dynamic $R_{DS(on)}$ due to trapped charges at surface interface impurities, bulk traps due to lattice mismatch are also not present.

- Breakdown Voltage independent of $R_{DS(on)}$
  With a properly designed drift layer doping concentration, the breakdown voltage of NexGen's Vertical GaN™ transistors increases with the drift layer thickness. Because of the absence of lattice mismatch in NexGen's GaN-on-GaN technology, drift layer thickness up to several tens of microns and breakdown voltages (BV) of ≥ 1200V – on par with the best SiC transistors - can be readily achieved.

As BV is mainly dependent on drift layer thickness and not on lateral Drain-Source distance as in GaN-on-Si devices and because in NexGen's Vertical GaN™ devices the $R_{DS(on)}$ contributions from the drift layer scales only sub-linearly with breakdown voltage, high breakdown voltage and low $R_{DS(on)}$ are no longer mutually exclusive design targets and enable fast switching GaN power transistors with ≥ 1200 V breakdown voltage

- Avalanche Breakdown
  Two main p-n junctions control the FET action in NexGen's Vertical GaN™ JFET in form of the gate-source and gate-drain diodes.
  In situations where the drain-source voltage exceeds the device breakdown voltage, avalanche breakdown can occur initially through the reverse biased drain-gate diode, subsequently causing the gate-source voltage to rise and open the channel.
  Contrary to lateral GaN-on-Si devices this is - within the limits of the devices' short term power dissipation capability and because the energy dissipation takes place in the bulk GaN (drift layer) and not on the sensitive device surface - a reliable mechanism to protect itself from transient spikes and other abnormal operating conditions, similar to Si-SJ and SiC devices.

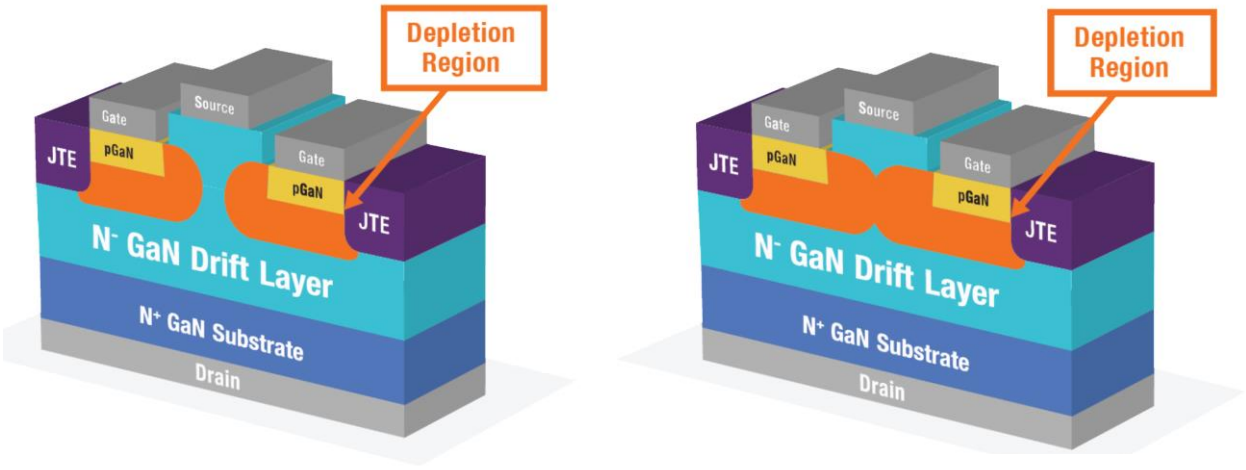
- No Crystal Lattice mismatch and Coefficient of Thermal Expansion mismatch
  Since Epi layers are grown homoepitaxially on a native GaN substrate, the crystal lattice structure and their rate of thermal expansion/contraction are perfectly matched throughout the entire die. Vertical GaN™ does not require buffer layers to isolate two different materials and hence the device does not suffer from performance limiting elevated defect densities and manufacturing challenges like wafer bow, warp and cracking. These potential reliability weaknesses and yield limitations do not exist in Vertical GaN™ devices, leading to increased reliability, yield and eventually reduced cost.

Attributes	GaN-on-Si	Vertical GaN™
Defect Density, cm^{-2}	10^9	10^3 to 10^5
Lattice Mismatch, %	17	0
CTE Mismatch, %	54	0
Layer Thickness, µm	1-2	> 40
Breakdown Voltage, (V)	600	4000V
OFF State Leakage	High	1nA (Low)
Avalanche Capability	No	Yes
Intrinsic Reliability	Low	High

Advantages	
Higher Yields	Lower cost
Higher Voltages	Broader range of addressable applications
Avalanche Capability	Avalanche tolerance is a key attribute for power devices
Higher Reliability	Broader range of addressable applications

Table 2 : Vertical GaN™ - Advantages of homoepitaxial grown GaN-on-GaN structures

- Improved Thermal Management
  All the losses in the Vertical GaN™ transistor are generated in the bulk of the device, either caused by the drain-source current or by currents to charge/discharge device capacitances. The device bulk is a very robust location compared to the sensitive surface of a lateral GaN. Contrary to lateral GaN devices, heat is transferred most optimally through homogenous material- without any additional layers - directly to the leadframe



$V_{gs} > V_t$ ➔ Channel open

V_{gs} =0V ➔ Channel is pinched OFF

Figure 3: Conceptual view of Vertical GaN™ channel control principle

Vertical GaN™ JFET Basic Operation and Properties

The NexGen Vertical GaN™ FET is a junction field effect transistor (JFET) in which the vertical n-GaN channel is sandwiched between two p-n junctions. The device cross-section bears some resemblance with FinFETs as used in silicon logic devices.

The bias difference between gate and source (V_{GS}) affects the extension of the depletion regions of the two p-n junctions into the n-GaN channel and controls the current between drain and source. When V_{GS} is below the threshold voltage (V_t), the JFET channel is closed. When V_{GS} is larger than V_t, the JFET channel opens and current can flow between source and drain.
Normally-ON (Depletion Mode) and Normally-OFF (Enhancement Mode) devices can be produced by modifying device design parameters.

The magnitude of effective gate voltage above V_t (V_{gt}= V_{GS} - V_t) affects the depleted n-type charge in the channel and thus the $R_{DS(on)}$ of the JFET. At higher V_{GS}, the larger V_{gt} causes a less depleted n-type charge and hence a lower $R_{DS(on)}$.

In this way the drain current is controlled by the gate source voltage and shows the familiar FET I_{DS}/V_{DS} relationship. $R_{DS(on)}$ is consequently also dependent on V_{GS} and increases when the voltage drop caused by I_{DS} along the source drain path is large enough to pinch the channel.

Figure 4

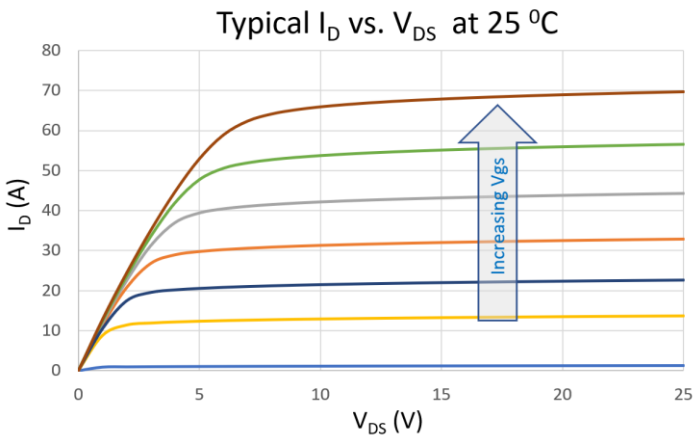


Figure 5

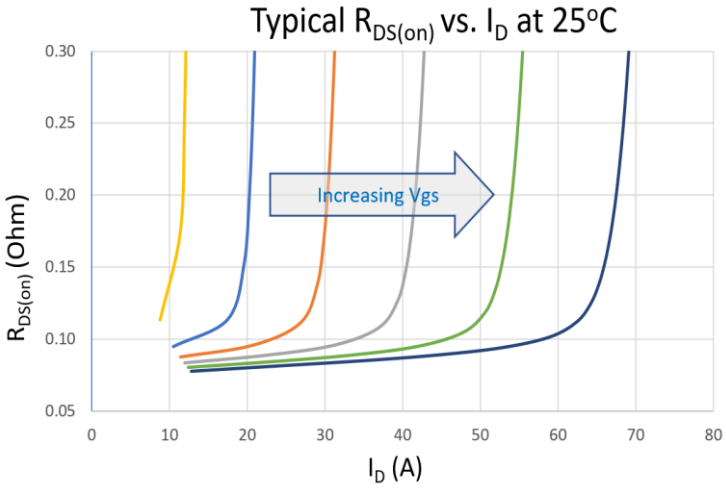


Figure 6

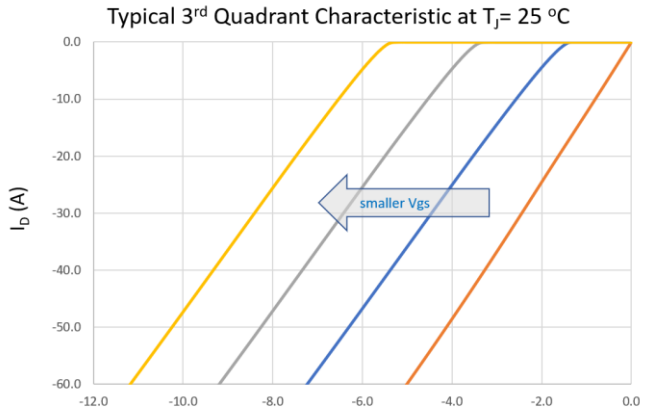
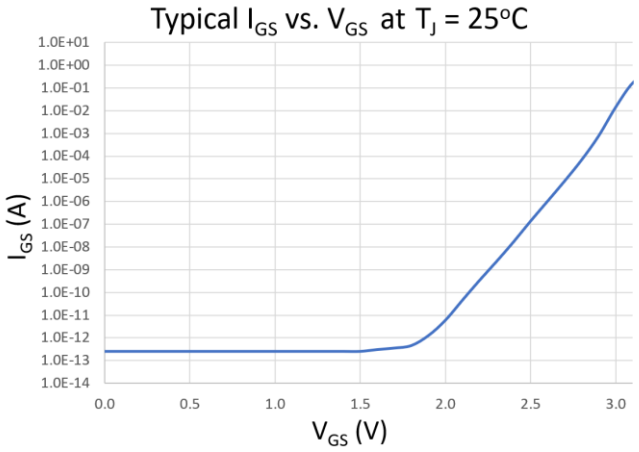


Figure 7



The Vertical GaN™ transistor construction, being essentially a majority carrier JFET device, does not create a parasitic body diode between drain and source as known from Si-SJ and SiC power MOSFET devices. Therefore Vertical GaN™ does not suffer switching losses caused by minority carrier/reverse recovery charge removal.

In addition, the device structure allows current flowing in reverse direction in case of a reversal of the drain-source voltage, in this way the JFET effectively assumes the function of a freewheeling body diode without the disadvantages of additional reverse recovery switching losses

The gate-source voltage necessary to reduce the depletion region and open the channel in enhancement mode devices is slightly forward

biasing the gate-source diode. This causes a small static gate current. The device is designed so that in normal operation only a few mili-amperes of static gate current is flowing.
It should be emphasized that the gate current itself does not enhance or otherwise control the channel current and therefore should be regarded as symptomatic of the "parasitic" gate-source diode but not necessary for the transistor device operation.

Figure 8

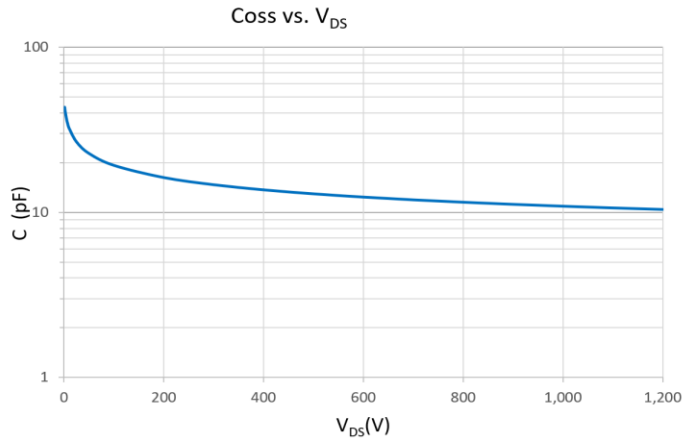


Figure 9

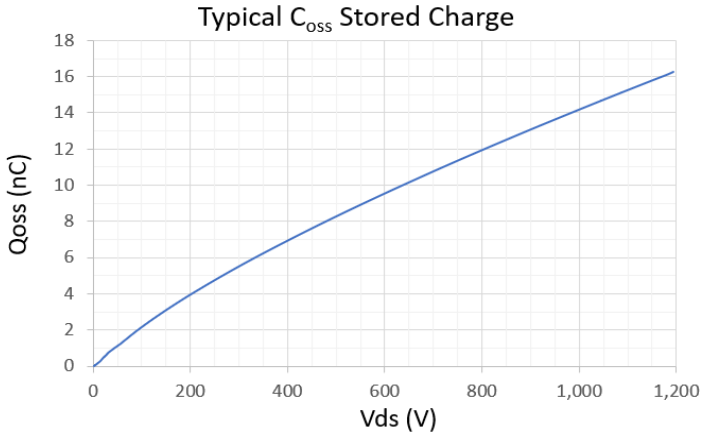
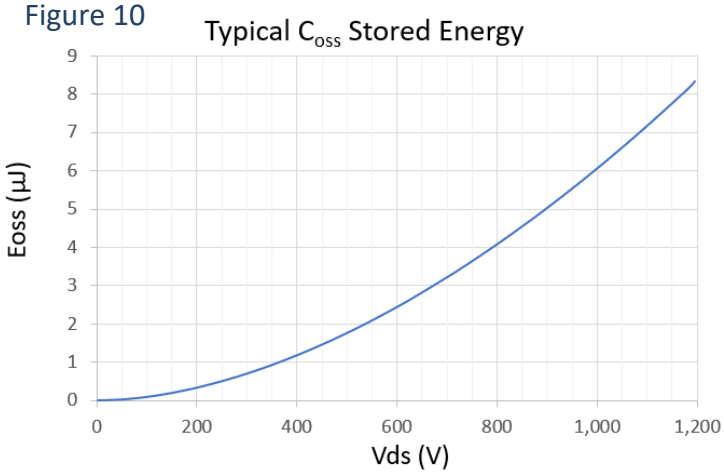


Figure 10



It is possible to overdrive the gate for a short amount of time in order to draw - e.g. during switching transitions - much more drain current than in normal operation. The gate source diode is sufficiently robust to accommodate the larger peak gate currents.

The small device area of NexGen's 1200V Vertical GaN™ technology leads to much smaller device capacitances compared to 1200V SiC devices at similar $R_{DS(on)}$ and drain currents. Vertical GaN™ based devices are also smaller than comparable lateral GaN devices with a much lower BV specification of 600V.
In particular, C_{oss} (and consequently Q_{oss} and E_{oss}) is very small, greatly reducing turn-on losses. This is key to the high efficiency and high switching frequency operation of applications enabled by Vertical GaN™ JFETs.

It should be noted that in NexGen's Vertical GaN™ JFETs the gate-source to gate-drain capacitance ratio is engineered to eliminate half-bridge hard-switching device re- turn-on even in extreme dv/dt situations

Summary

NexGen's Vertical GaN™ technology combines device properties previously believed to be incompatible and therefore impossible to achieve:

- Devices with superior switching frequency and very high breakdown voltage
- Avalanche robustness better than silicon SJ MOSFETS and SiC devices with switching frequencies of GaN devices
- Mass production cost scalability with advanced device and material properties

Vertical GaN™ delivers the promise of GaN materials without being subjected to the reliability and cost compromises inherent in the construction of lateral GaN-on-Si devices. Figure 11 shows how the unique combination of the Vertical GaN™ power device allows a single technology to address the full range of power conversion applications that currently can only be served by a multitude of technologies. More importantly, as shown in Table 4, NexGen's Vertical GaN™ technology enables circuit and system designers to eliminate design constraints normally encountered with devices of traditional technologies. Thus, new generations of smaller power systems with higher efficiency are now possible

Figure 11 Vertical GaN™ serves the entire power device market

	Vertical GaN (GaN-on-GaN	Lateral GaN (GaN-on-Si)	SiC	Si SuperJunction	IGBT
Switching Frequency	✓✓✓✓ (>> 1 MHz)	✓✓✓ (~1MHz)	✓✓ (several 100KHz)	✓✓ (~250KHz)	✓ (50KHz)
Breakdown Voltage (BV)	> 1200V	approx. 650V	> 1200V	< approx. 900V	> 1200V
Switching Losses	Very low	low	high	high	high
Qrr	0	0	low	high	0
Avalanche	robust	no Avalanche	ok	ok	ok/robust
Reliability	high	medium	high	high	high
Cost	low	high	moderate	low	low

Table 4 : Vertical GaN™ outperforms traditional power switch technologies