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# Avalanche Capability of Vertical GaN p-n Junctions on Bulk GaN Substrates

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***Abstract*— Inductive avalanche test results presented in this letter demonstrate that GaN p-n diodes can sustain single-pulse and repetitive inductive avalanche currents. The 0.36 mm$^2$ vertical GaN p-n diodes can sustain single-pulse avalanche currents as high as 10 A. The safe zone of the single pulse avalanche current is limited by peak pulse power and energy deposited in the device. The temperature dependent behavior of the breakdown voltage and the reverse-voltage at onset of avalanche has a positive temperature coefficient. Repetitive avalanche ruggedness testing was performed by applying 10$^5$ pulses at 5 kHz frequency with increasing repetitive stress current. Based on a population of 63 devices, the incremental failure rate under repetitive avalanche current increases with increasing avalanche current. The devices that survive the step stress test sustain no parametric drift under repetitive avalanche.**

***Index Terms*—Bulk GaN, PN diode, avalanche, avalanche ruggedness, vertical power semiconductors.**

## I. Introduction

GaN power semiconductor devices have been the recent focus of intense development efforts due to the promising material properties of GaN material system [1-3]. Among the various possible approaches to GaN power electronics, vertical devices on native GaN substrates offer the advantage of better area efficiency due to ability to grow thick drift regions and improved reliability due to the reduced defect density and the possibility of field control via doping profile optimization. For power switching and rectifying applications, the ruggedness in breakdown is a critical requirement as supplementary snubber circuits impose a performance and efficiency penalty on the system [4-6].

Earlier work has demonstrated vertical GaN p-n junction diodes grown on GaN substrates with performance close to the Baliga figure-of-merit (FOM) limits [7, 8]. The reverse bias testing in earlier GaN p-n diode studies have been limited to the observation of leakage and breakdown under quasi-static conditions under resistive load [7, 8]. Despite the fact that positive temperature coefficient of the breakdown voltage has been observed from quasi steady-state breakdown studies, the peak current densities have been necessarily small due to the long pulse times involved. In this paper we demonstrate inductive avalanche capability and ruggedness of vertical GaN p-n junction diodes for the first time.

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## II. Experimental

GaN p-n junction diodes were grown by metal organic chemical vapor deposition (MOCVD on native GaN substrates grown by hydride vapor phase epitaxy (HVPE) and fabricated using procedures that were described earlier [7, 8]. The diodes were packaged in molded TO-220 packages. The doping and the thickness of the drift region were adjusted to target a breakdown voltage around 1000 to 1100 V. This low breakdown voltage was necessary to make sure that the breakdown voltage of the device under test will be lower than the breakdown voltage of the switch used in the test setup. The junction termination extension of the GaN diode enabled a breakdown voltage close to the design limits as in earlier reports. The devices under study had an active area of 0.36 mm$^2$ with a median ON state resistance of 0.5 Ohms. The median value of the ON resistance was impacted by the backside ohmic contact resistance and silver-filled epoxy resin die-attach material. The devices exhibited a median ON voltage of 3.0 V and 3.6 V at forward currents of 10 mA and 1A, respectively. Parametric testing of the devices was performed by using FocusTest FTI-1000 tester (ATE), and devices passing breakdown voltage and ON resistance criteria were accepted for avalanche testing.

Temperature dependent measurements of breakdown voltage under constant reverse current were made using a Keithley 2657A source-measure unit (SMU). The temperature dependent breakdown voltage and avalanche voltage measurements were made by attaching the device to a temperature controlled heat sink, and the device temperature was measured continuously through-out each temperature dependent test for each device by means of a thermocouple attached to the TO-220 package tab.

The avalanche testing was done on a custom built unclamped inductive switching (UIS) test setup whose schematic is shown in Fig. 1. The setup employed a SiC metal-oxide-semiconductor transistor with breakdown voltage of 1700 V to control the inductor current.

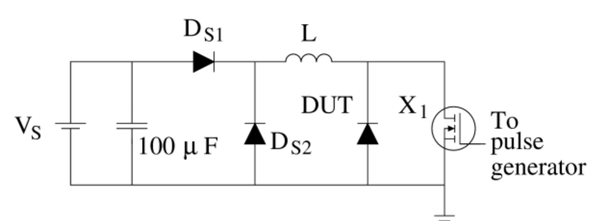


Figure 1) Avalanche test circuit. $D_{S1}$ and $D_{S2}$ are Schottky diodes, $X_1$ is the switch with the gate controlled by an external pulse generator. L is the load inductor and the DUT is the device under test.

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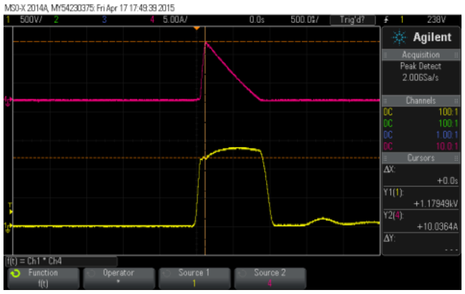
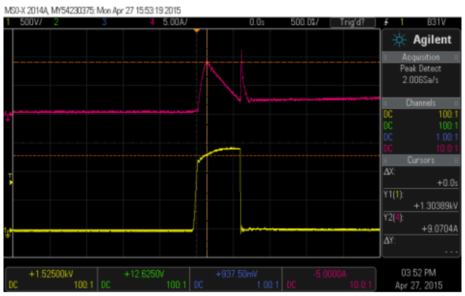



(a)




(b)

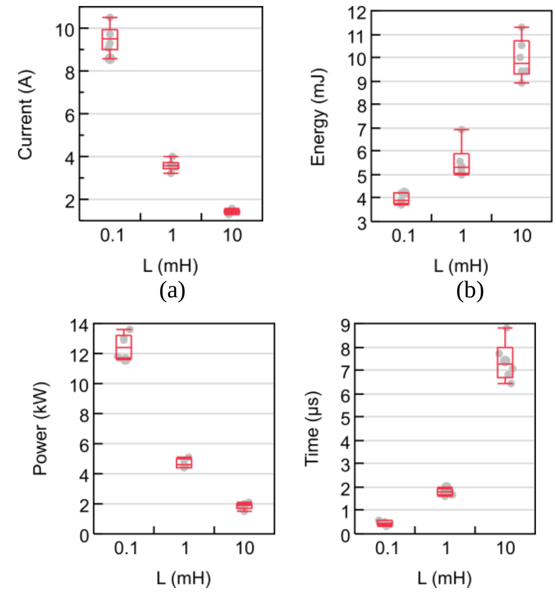
Figure 2: Scope waveforms displaying DUT current (purple) and the voltage (yellow): a) normal avalanche, and b) destructive avalanche

Repetitive avalanche testing was performed by applying periodic avalanche current pulses to the device at a repetition rate of 5 kHz for $10^5$ times. In order to test the limits of repetitive avalanche ruggedness, the repetitive avalanche current was increased in a step stress manner after each set of $10^5$ pulses. For this test, devices were individually mounted to a forced air cooled heat-sink. Parametric testing of the devices was performed on incoming devices and after each step of repetitive avalanche testing.

## III. RESULTS AND DISCUSSION

Figure 2 presents the avalanche waveforms as captured from the oscilloscope screen for two different devices under 100 µH load inductor. Figure 2a is a normal avalanche waveform demonstrating that the device can sustain single pulse avalanche currents up to 10 A. In contrast, Fig. 2b is a destructive avalanche waveform for a similar device. As seen from both figures, the device voltage at the peak avalanche current exhibits an initial plateau followed by a gradual increase despite the fact that avalanche current is decreasing. We attribute this increase in the device voltage to the heating of the device as a result of energy deposited within the active region. We will refer to the value of the device reverse voltage at the peak of the avalanche current as the avalanche voltage ($V_A$). The destructive avalanche waveform shown in Fig. 2b indicates that the damage does not occur at the beginning of the current pulse, but after dissipation of some amount of energy as would be consistent with a thermally induced destruction of the device. In Fig. 2b we define the time from the onset of the avalanche to the destruction of the device as breakdown-time.

Figure 3 presents the avalanche pulse parameters that resulted in device destruction using 100 µH, 1 mH, and 10 mH inductors for 6 devices each. For the tests shown in Fig. 3, the inductor current was increased by manually adjusting the DC power




(a) (b) (c) (d)

Figure 3) Distribution of various pulse parameters for the smallest current pulse that results in device destruction: a) peak inductive avalanche current, b) Energy deposited into the device, c) Peak power dissipated on the device, and d) Time to onset of breakdown

supply voltage in small increments and triggering a single pulse while waiting at least 1 minute between consecutive pulses. Figure 3 demonstrates that avalanche capability is not limited to a few select devices and exhibits the range of variation in the single pulse avalanche capability within this manufacturing lot. From Fig. 3, it is observed that the devices can handle avalanche currents as large as 10 A (2.8 kA/cm$^2$). The charts in Fig. 3d define the single-pulse safe operating zone under inductive avalanche conditions. The reduction in energy that can be deposited in the device with increasing peak power indicates that the avalanche capability is strongly impacted by the transient nature of the heat transfer.

Figure 4 presents the temperature dependence of the breakdown voltage ($V_R$) as measured by a K2657A SMU, and the avalanche voltage ($V_A$) as measured on the avalanche test system using a 1 mH inductor. As can be seen, all curves exhibit a positive temperature coefficient close to 1 V/K. Figure 4 validates the identification of quasi steady-state breakdown as

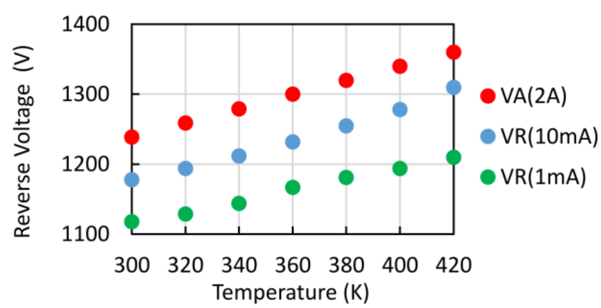



Figure 4: Breakdown voltage ($V_R$) and avalanche voltage ($V_A$) as a function of temperature. Breakdown voltage $V_R$ is the reverse voltage measured using an SMU under 1mA and 10mA reverse current. The avalanche voltage is measured under 2 A peak inductive pulse supplied from a 1mH inductor.

avalanche in earlier measurements as was described in

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references [7, 8].

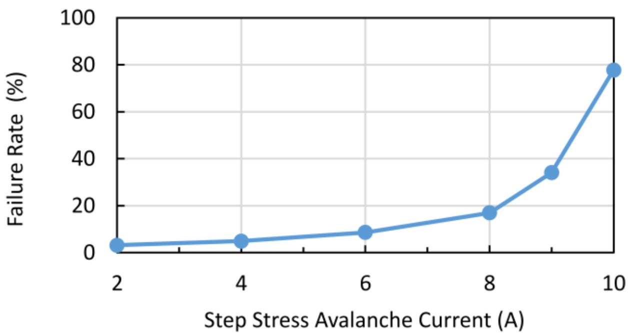


Figure 5a) Incremental failure rate at each test step

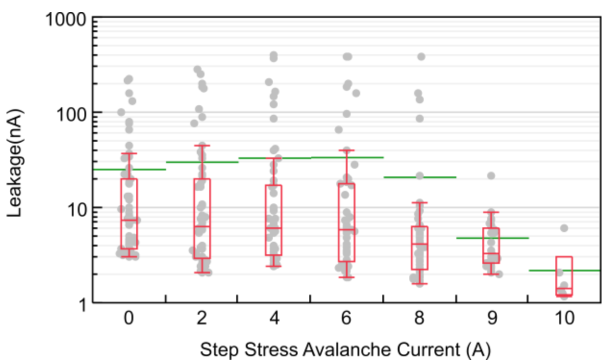


Figure 5b) Statistics of reverse current at a reverse bias of 600 V for devices surviving after each repetitive avalanche stress step. "0A" indicates incoming population. The plot shows the reverse current for individual devices with dots, the box-plot and the mean line.

Figure 5 provides information about the avalanche ruggedness of 63 devices selected based on the criteria of passing a post-packaging breakdown voltage test without further screening. The step stress test was performed as described earlier in Section II. From Fig. 5a it can be seen that the incremental failure rate is increasing with repetitive stress current and reaches 77% at 10A. For the devices that survive and continue with the testing, the forward voltage, ON resistance and breakdown voltage do not exhibit any significant shift. The statistical analysis of reverse leakage at reverse voltage of 600 V, shown in Fig. 5b, indicates that the mean and median of the surviving population is decreasing at high repetitive stress currents due to the, elimination of devices with higher leakage current. This observation suggests that reverse leakage at high reverse bias voltage can be used as a screening criteria for devices that are required to have repetitive avalanche ruggedness. Given the large number of pulses and the high repetition frequency, the results presented in Fig. 5 can be considered to suggest that the GaN p-n devices are robust and stable under repetitive avalanche condition until the limits of the single pulse safe zone are exceeded.

## IV. CONCLUSIONS

Inductive avalanche capability and ruggedness characterization of vertical GaN p-n junction diodes grown on native GaN substrates are presented for the first time. The results indicate that the reverse breakdown is due to avalanching. The devices can sustain currents as high as 10 A (2.8 kA/cm$^2$) and sink in energy as high as 10 mJ under inductive avalanching conditions. The ruggedness tests show that the devices surviving the repetitive avalanching do not show parametric drift.

## V. ACKNOWLEDGEMENTS

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