1.5-kV and 2.2-mΩ-cm^2 Vertical GaN Transistors on Bulk-GaN Substrates

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***Abstract*— In this letter, vertical GaN transistors fabricated on bulk GaN substrates are discussed. A threshold voltage of 0.5 V and saturation current >2.3 A are demonstrated. The measured devices show breakdown voltages of 1.5 kV and specific ON-resistance of 2.2 mΩ-cm^2, which translates to a figure-of-merit of V_{BR}^2/R_{ON} ~1 × 10^9 V^2 Ω^{-1} · cm^{-2}.**

***Index Terms*— Gallium nitride, vertical transistors, power semiconductor devices.**

I. Introduction

THERE is a great interest in developing switching power devices based on wide bandgap materials [1]–[9], such as silicon carbide (SiC) and gallium nitride (GaN) since silicon power devices are approaching material physical limits. The theoretical material property based power device figure-of-merit of GaN is significantly better than Si [1]. To date, a majority of the GaN power device development effort has been directed toward lateral devices, such as high-electron mobility transistors (HEMTs), fabricated in thin layers of GaN that are grown on foreign substrates. Some well-known issues include current-collapse, dynamic on-resistance, and inability to support avalanche breakdown [2]. By fabricating power semiconductor devices on bulk GaN substrates, it is expected to be possible to realize the material limit potential of GaN including true avalanche breakdown capability and to create vertical architectures that can do not suffer from thermal management issues associated with thin film surfaces, and provide increased number of die on a wafer.

Vertical GaN diodes with breakdown voltages up to 3.7 kV have been fabricated on bulk GaN substrates [7], [8], [10]–[12]. However, due to the low availability of suitable substrates and process complexities such as a lack of selective area doping, it has been challenging to demonstrate high performance vertical GaN transistors [13]–[16].

In this letter, we report on vertical GaN transistors with breakdown voltages of 1.5 kV fabricated on pseudo-bulk GaN substrates. The transistors have a positive threshold voltage and exhibit a specific on-resistance of 2.2 mΩ-cm^2.

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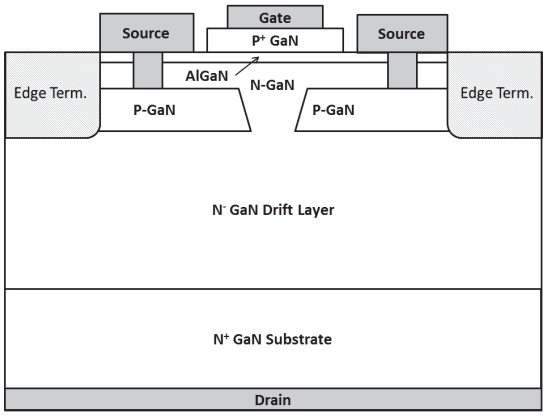

Fig. 1. Schematic cross-section the vertical GaN transistor on bulk GaN.

II. Growth and Fabrication

The necessity of growing GaN on mismatched substrates such as sapphire, silicon, and silicon carbide creates difficulties for vertical device structures and results in poor material quality with high defect densities. In this letter, high performance vertical GaN power transistors have been achieved through homoepitaxial growth on GaN substrates and through the development of processing techniques applicable to the vertical p-n devices and their edge termination [17]–[20].

A schematic cross-section diagram of a vertical GaN transistor is shown in Fig. 1. The GaN layers comprising the p-type blocking layers and the vertical drift region were epitaxially grown by metal-organic chemical vapor deposition (MOCVD) on 2-inch bulk GaN substrates. Imaging plan-view cathodeluminescence (CL) reveals that the threading dislocation density in the films grown over bulk GaN substrates is 10^4 cm^{-2}, or at least 4 orders of magnitude lower than for GaN films grown on Si or SiC substrates. The maximum breakdown voltage of the device is determined by the design of the n-type drift-layer layer doping and the thickness. The nominal drift region net doping density for the devices in this study is N_D-N_A = 1 × 10^{16} cm^{-3}, while the drift layer thickness is 15 μm. The p-region is realized by in-situ growth of Mg-doped p$^+$ GaN epitaxial layer on top of the n-type GaN epitaxial drift region. Narrow trenches were etched using a Cl-based chemistry in an inductively coupled plasma (ICP) process. An n-type GaN layer was regrown to fill the trenches and form

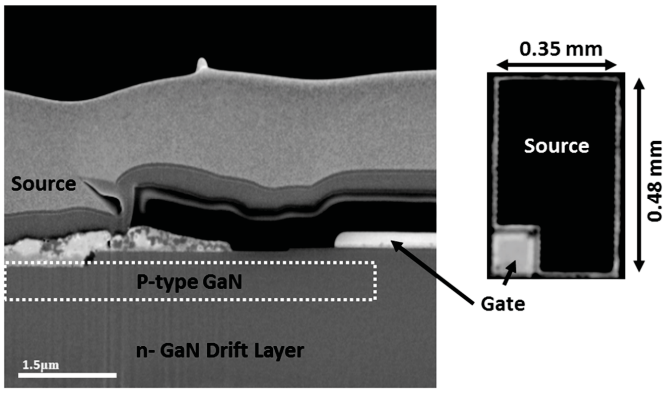

Fig. 2. Transistor cross section and top view image.

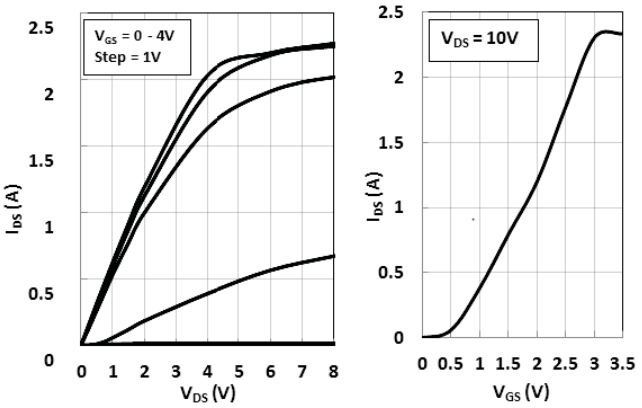

Fig. 3. DC output and transfer characteristics of the vertical GaN transistor.

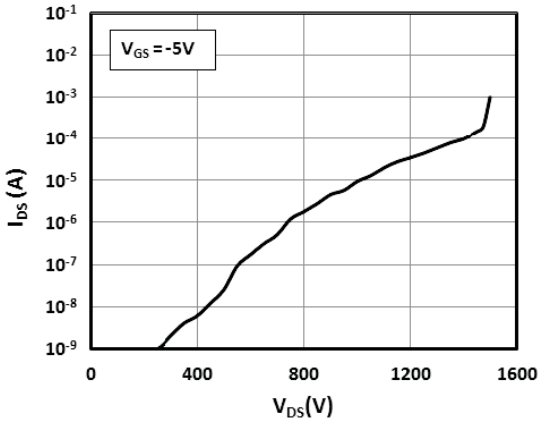

Fig. 4. Reverse current-voltage characteristics of the vertical GaN transistor.

a channel above the patterned p-type GaN layer. The n-type layer was capped by an AlGaN layer with 20% Al content. The AlGaN/GaN interface resulted in a 2DEG channel due to polarization induced charge at the hetero-interface. Finally, the p-type GaN layer was deposited and patterned to form the top gate. The thickness and doping of the p-GaN layer in the channel region, and the charge at the AlGaN/GaN interface were designed to result in a positive threshold voltage.

The buried p-body layer can be contacted using an appropriate metal for ohmic contact to p-type GaN, such as Pd, Pt, or Sc. In these devices, a Sc/Au stack was utilized. The source electrode was Ti/Al based. The source electrode overlapped with the buried p-body electrode to minimize the cell pitch. The contact to the buried p-GaN and the Ti/Al source electrode were simultaneously subject to a rapid thermal anneal. The gate electrode was also Sc based and was separately annealed. A 500 nm thick SiN_x film serving as an inter-layer dielectric (ILD) was deposited by plasma-enhanced chemical vapor deposition (PECVD). Via contact holes were patterned for both the source and the gate. Finally, 4 μm thick source and gate pad metals were deposited for wire bonding and current spreading. A backside contact (drain) was formed by evaporating aluminum onto the bottom of an n^+-type GaN substrate. The SEM cross section and chip dimensions are (0.35mm $\times$ 0.48mm, active area is 0.15 mm^2) shown in Fig. 2.

III. Measurement and Discussion

In order to obtain a positive threshold device, the positive charge in the p-GaN top gate layer, the charge in the polarization induced 2DEG, the doping in the n-type channel layer, and the proximity of the buried p-GaN layer must be balanced. The maximum allowable positive gate swing allowed for a GaN p-n diode gate is approximately 3 V before the onset of significant current flow. These devices typically exhibited a gate current of approximately 4 mA at $V_G = 3$ V. A maximum threshold target of 1.8 V was desired to provide sufficient gate swing to fully open the channel so that the on-state resistance is not severely compromised. For a normally off power device, which was the intended target of this design, the positive threshold should be high enough so that off-state current is minimized at the rated blocking voltage. The length of the channel region was chosen to be sufficient to preclude the effect of the drain voltage on the potential barrier in the channel in the off-state. Fig. 3 shows the output and transfer characteristics of the device in this study. This device has a linearly extrapolated threshold voltage of 0.5 V, and has a saturation current greater than 2.3 A. The active area is 0.15 mm^2 which translates to a current density of 1.5 kA/cm^2. A differential specific on resistance of 2.2 mΩ-cm^2 is calculated based on resistance measurements and the active area given.

The reverse characteristics of the transistor are shown in Fig. 4. The measurement was performed on-wafer using a temperature stage and needle probes. The breakdown voltage (at 1 mA) is 1.5kV at T = 300°K. The edge termination scheme used in the transistors here are similar to those in the p-n junction diodes that operate in the avalanche region [10]–[12], [17]. However, we can't be certain that the breakdown is due to avalanche. The topic is being studied and results will be published in the future.

Combining the measured breakdown voltage and the specific on resistance translates into a power device figure-of-merit [21] of $V_{BR}^2/R_{ON} = 1.0 \times 10^9$ $V^2 \cdot \Omega^{-1} \cdot cm^{-2}$.

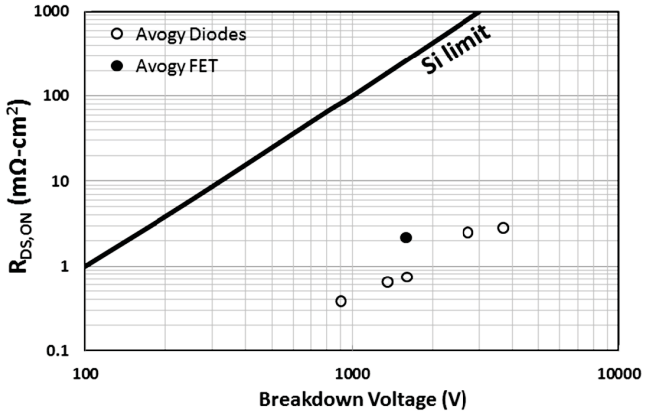

Fig. 5. Power device figure-of-merit comparison of this study to Si theoretical limit. Also shown are the previous Avogy vertical diode results.

Figure 5 depicts the placement of this data point on the power device figure-of-merit chart along with our earlier diode results. The diode results serve to illustrate the gap between this FET and the best measured bulk GaN p-n diodes. Clearly, much optimization work is needed to cover the performance gap.

IV. Conclusions

Vertical GaN transistors using bulk GaN substrates were fabricated. These transistors exhibit larger than 2.3A saturation current, breakdown voltages of 1.5kV, area differential specific on-resistance of 2.2 mΩ-cm^2, and a FOM of 1.0×10^9 V$^2 \cdot \Omega^{-1} \cdot$ cm^{-2}. Some critical and differentiating features of the device presented here are the use of a junction termination extension scheme (rather than field plates or simple implant based isolation) and the shorting of the buried p-GaN layer to the source contact. The results are encouraging for vertical GaN-based device architectures to increase performance of future high power electronics systems. Future optimization work will focus on improving the edge termination, substrate thinning to reduce resistance, and reducing leakage currents.

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