GaN is Great, True GaN™ is Better!

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This article describes benefits of Gallium Nitride (GaN) and True GaN™ technology for power electronics industry.

Revision 1.4

avogy

1. Gallium Nitride and Power Systems—A Match Made in Heaven

We live in a world of electronics – computers, tablets, phones, LED lighting, TV, audio, gaming systems, household appliances, and electric and gas powered vehicles. With the advent of Internet of Things (IoT), the digital era of connected world is here. These electronic systems need power. Electrical power goes through many transformations or conversions at multiple points in its journey from generation in turbines, to transmission in high voltage lines to its distribution to the outlets in our homes. It is a multi-billion dollar and rapidly growing industry. As such, there is a global drive to improve the efficiency with which electric power is generated, distributed, and converted.

As consumers, we're all too familiar with the power adapters that plug into the wall. These gizmos convert power from AC (alternating current) to DC (direct current). Power converters or adapters are ubiquitous and come in all shapes and sizes. Some are external (e.g. laptop), whereas others are neatly tucked away inside the system (e.g. TV). Even within a given power system, various sub-systems have different DC operating voltage requirements. Innovation in creating a better converter would greatly benefit all aspects of any power systems.

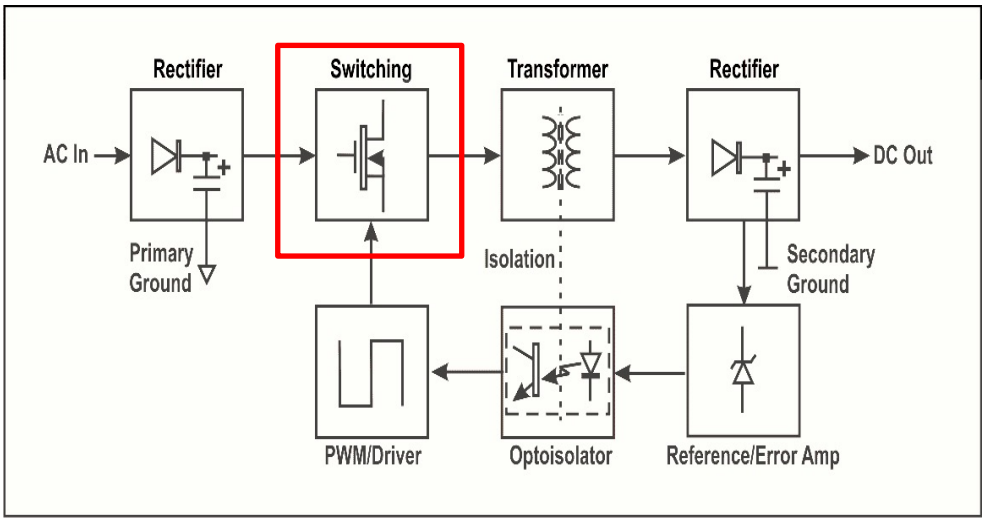


Figure 1 Block diagram of SMPS based AC-to-DC power converter. Semiconductor switch is the key element in this system.

Power electronics employs solid-state devices to process or convert electrical power—input power is processed with some control to produce conditioned output power. Most converters today are *Switch Mode Power Supplies* or SMPS. They turn input power at a given voltage and current to output power at a different voltage and current. This transformation is done by storing input energy in components called capacitors and inductors, then chopping that energy up into packets using a semiconductor switch, and then changing these packets of energy to a different voltage and current using a transformer.

Converters can broadly be classified as: *dc-to-dc converter* (dc input voltage converted to dc output voltage with smaller or larger magnitude), *ac-to-ac rectifier* (ac input voltage is rectified to produce dc output voltage), or *ac-ac cycloconversion* (ac input voltage is converted to a given ac output voltage of different magnitude and frequency).

Figure 1 shows a block diagram of SMPS based ac-to-dc converter. Capacitors, inductors and transformers are considered passive components. In SMPS, these components are physically large. The semiconductor switch that performs the energy chopping function is the key element in this system. It sees high current flow and power losses that manifest as heat. Heat generated from the conversion losses, along with the inductors and capacitors, dictates the size of SMPS and makes them physically large. An ideal SMPS would weigh nothing, have no volume, and incur no losses when it does its power conversion.

To reduce the size of SMPS, we have to operate at high frequencies. Passive components such as inductors and capacitors make up the bulk of power system volume. Operating at high frequencies allows the reduction in their size. However, in order to operate at high frequency, we need a better switch – one that can run at MHz (10^6 or million Hz) frequencies. For the last three decades, silicon power devices (MOSFETs, IGBTs, and diodes) have dominated the power device market. Although there have been tremendous improvements in silicon power device performance, they are now approaching the physical limits of silicon. Silicon-based switches can only operate in the kHz (10^3 or thousand Hz) range. Thus, high frequency power semiconductor switches are key to enable high efficiency power conversion. The potential cost savings from increased efficiency could be in the hundreds of billions over the next decade.

Power semiconductor devices have historically been fabricated from silicon (Si) and more recently, silicon carbide (SiC). There is great interest in developing gallium nitride (GaN) power devices because they can far exceed the performance of silicon-based devices, which will allow substantial improvement of the efficiency of power electronics. The fundamental material limits of GaN are nearly 4X better than SiC and over a 1,000X improvement over Si. There are three main types of GaN available today: GaN-on-Si, GaN-on-SiC and GaN-on-GaN. True GaN™ technology is based on GaN-on-GaN substrates.

In addition to the frequency of operation, power semiconductor switches can be appraised on the basis of two other important performance indicators: breakdown voltage and ON-state resistance. Breakdown of semiconductor is a phenomenon by which the device can no longer support high voltage across two terminals in a non-conducting or OFF state. ON-state resistance is the resistance between two terminals in a conducting state. Ideal power

semiconductor would have infinitely high breakdown voltage and zero resistance between the two terminals in a conducting or ON-state.

ON-state resistance can be scaled down by using larger chips. However, breakdown voltage and frequency are innate material qualities. Figure 2 shows the market segmentation by maximum breakdown voltage and frequency. True GaN™ has a unique advantage in high performance (high voltage and high frequency) and with minimal effort, it is capable of competing in other markets with ease.

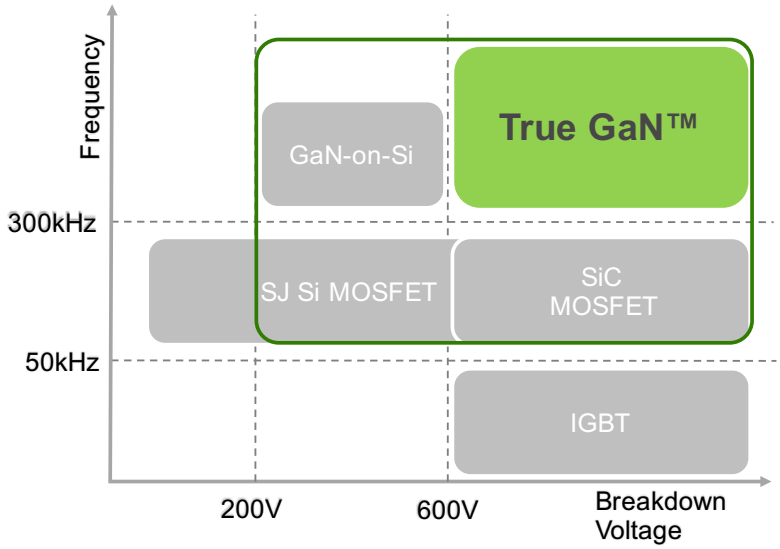


Figure 2 Power electronics market segmentation by breakdown voltage and frequency. True GaN™ can dominate in other areas beyond the high performance space.

Table 1 presents a comparison of key material properties pertaining to power semiconductor devices. Bandgap is energy difference between conduction and valence band of semiconductors. Higher bandgap materials can operate at higher temperatures and withstand higher voltages before breakdown occurs. SiC and GaN both fall into a class of semiconductors referred to as Wide Bandgap semiconductors. GaN has a 3X advantage over Si and it is also better than SiC. In electron-based unipolar devices, higher peak electron velocity enables higher switching frequency. Higher frequency enables reduction in size of passive components like inductors, transformers and capacitors in power conversion systems.

Critical electric field is the property of semiconductor device that determines the voltage at which breakdown occurs. Materials with higher critical electric field are capable of operating at higher voltages at lower thickness or distance between two terminals in OFF-state. Lower thickness results in lower resistance between the same terminals in the ON-state. Critical electric field of GaN is significantly better than SiC and Si.

Table 1: Comparison of GaN with Si and SiC

Parameter	Symbol	Unit	Si	SiC	GaN
Bandgap	E_c	eV	1.12	3.2	3.43
Relative Dielectric Constant	ϵ_s	-	11.9	10	9.5
Electron Mobility	μ_n	$cm^2/(V.s)$	1500	700	2000
Peak Electron Velocity	v_{peak}	10^7 • cm/s	1	2	2.5
Critical Electric Field	E_c	MV/cm	0.3	3.0	3.3
Baliga Figure of Merit (BFOM)	$\epsilon_s \mu_n E_c^2$	W/cm^2	1	392*	1416*

* Normalized to Si

Baliga Figure of Merit (BFOM) is a unified figure of merit for power semiconductor device as it simultaneously takes into account both the critical electric field and mobility properties of materials. Higher BFOM means that devices are capable of operating at higher frequencies at high voltage. Table 1 shows BFOM normalized to the value of Si to show the relative advantages of materials. GaN is over 1000x better than Si and nearly 3x better than SiC.

In summary, for high efficiency power electronics systems, GaN offers unprecedented advantages over Si and SiC. High voltage operation at significantly higher frequencies with extremely low conduction losses results in:

- Increased efficiency
- Reduction in size of passive components at higher frequency and thus reduced overall system size, weight and cost

Avogy's resonant circuit topologies and control circuits are designed to achieve lossless switching by fully exploiting the benefits of True GaN™ technology. The True GaN™ platform makes it possible to build the smallest, lightest and most efficient power systems on the planet. This platform is the foundation of Avogy's first product—Zolt line of AC/DC adapters that are now in the market. This platform will also be extended to design modules for other stages of power conversion.

3. True GaN™ Technology

Epitaxy is the technique of atomically growing a crystal, layer by layer, on the surface of another crystal. Homoepitaxy refers to growth where a crystal is grown on a substrate of the same material. Gallium nitride (GaN) devices can be created on epitaxially grown GaN layers on different types of carrier wafers. Thus GaN wafers can be classified by the type of carrier wafer used to epitaxially grow GaN. Figure 3 shows the three main types of GaN substrates available today. GaN-on-Sapphire is also available but it has not been widely adopted.

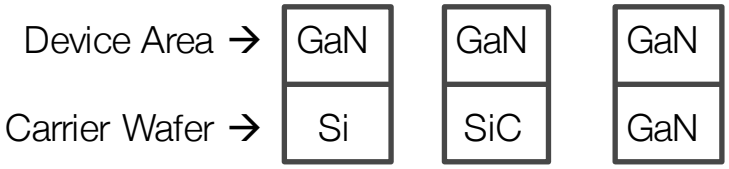


Figure 3: Different types of GaN substrates

To realize the full potential of the superior material properties of GaN, homoepitaxially grown GaN substrates are a superior approach for fabricating vertical power devices. Therefore, True GaN™ technology is based on GaN-on-GaN substrates.

Table 2: Comparison of different types of GaN substrate

Device Area → / Carrier Wafer →	GaN / Si	GaN / SiC	GaN / GaN
Attribute	GaN-on-Si	GaN-on-SiC	GaN-on-GaN
Defect Density [cm^{-2}]	10^9	$5x10^8$	10^3 to 10^5
Lattice Mismatch [%]	17	3.5	0
CTE Mismatch [%]	54	25	0
Layer Thickness [µm]	1-2	2-6	> 40
Reliability	Low	Low	High
Device Types	Lateral	Lateral	Vertical & Lateral

Table 2 provides a comparison of different GaN substrates. In order to appreciate the difference between various GaN substrates, a brief discussion on crystal structure is warranted. Lattice or crystal structure is a unique arrangement of atoms in a crystalline semiconductor. Lattice constant

characterizes the spacing between two atoms in this highly ordered structure. GaN-on-Si and GaN-on-SiC are considered heteroepitaxial structures as they involve assimilation of two different lattice structures, namely GaN and Si or GaN and SiC. GaN-on-GaN substrates are homogenous.

Major disadvantage of epitaxial growth of GaN on Si or SiC carrier wafers stems from the lattice constant mismatch of the two material systems. Mismatched lattice structures cause high stress in the epitaxial layer of GaN being grown on the top. This leads to defects in the crystalline structure known as dislocations. These dislocations alter and degrade the electrical properties of GaN and are the source of lower breakdown voltages. Even more importantly, they are the source of poor reliability of these devices under stress.

Epitaxially growing thick (>10µm) device layers on materials with mismatched lattice and coefficient of thermal expansion (CTE) results in wafer bow, warp, and cracking. In case of GaN-on-GaN, both lattice and CTE are perfectly matched. As a result, very thick layers of GaN can be epitaxially grown on bulk GaN substrate which enables the fabrication of high breakdown voltage devices. Avogy has demonstrated the growth of 40µm GaN layers and >4000V breakdown voltage diodes.

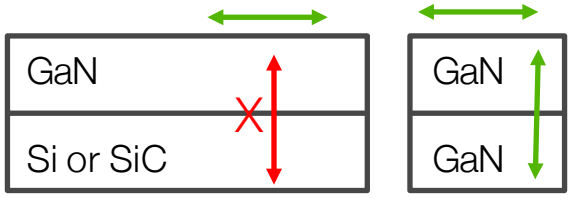


Figure 4: GaN-on-GaN enables creating vertical devices whereas heterostructures are limited only to large area lateral devices.

One major advantage of GaN-on-GaN over GaN-on-Si (or GaN-on-SiC) is the possibility to create vertical devices as shown in Figure 4. GaN-on-Si devices can only be fabricated laterally where the GaN material exists. For achieving higher BV for GaN-on-Si, device area increases greatly which reduces yield and increases die cost.

Homoepitaxial growth on GaN substrates requires polished surfaces cleaved along specific crystallographic axes at desired angles (referred to as ‘offcut’ or ‘miscut’). The offcut surface presents atomic bonds that help initiate epitaxial growth on the substrate. Proper choice of offcut angle is necessary for good morphology. Morphology is a description of the three dimensional shape, size, texture and phase distribution of surface. An optimal choice of offcut results in defect-free (no hillocks or local bumps) GaN layer with minimal RMS roughness. It also impacts dopant incorporation in the growth layer which can in turn impact the device performance negatively.

Avogy has patented the most optimal spectrum of these offcut angles that results in best morphology and thus best device performance. Using optical profilometer scans of wafers, Avogy has been able to create models to correlate offcut angles to yield. This provides us predictive power on incoming wafers during manufacturing. To date, Avogy has successfully demonstrated growing extremely thick (40μm) using our patented technique. Additionally, since its inception in 2011, Avogy has worked closely with all bulk GaN substrate vendors to validate growth and regrowth techniques across variety of different bulk GaN substrates manufactured via different processes.

There are two types of layers are used to fabricate semiconductor devices, a n-type doped GaN layer (n-GaN) and p-type doped GaN layer (p-GaN). Avogy has developed homoepitaxial process to produce ultra-low doped n-type GaN layers (n-GaN). This n-GaN layer is a critical component of our device in order to produce high breakdown voltages. In the epitaxial growth of n-GaN on top of a p-GaN layer, a commonly encountered problem is magnesium (Mg) memory effect. Mg is a p-type dopant used in GaN. Mg tends to linger around and produces an undesirable tail effect in n-type GaN layers. Avogy has also developed techniques to control the Mg memory effect. This gives us the ability to grade p-n junctions or to produce sharp p-n junction profiles as desired.

Homoepitaxy on flat surfaces is challenging but 3-D structures present an added level of challenge. Post-epitaxy holes and trenches need to be completely planarized. Avogy has developed highly planarizing regrowth process for n-GaN on n-GaN and p-GaN on p-GaN with very low surface roughness.

In summary, the salient features of True GaN™ technology:

- Homoepitaxial growth on GaN substrate
- Patented the most optimal spectrum of these offcut angles that results in best morphology and thus best device performance.
- Flexibility to use bulk GaN substrates from all major vendors
- Ability to produce ultra-low doped n-GaN
- Proprietary methods to control Mg doping during growth to grade p-n junctions or to produce sharp p-n junction profiles as desired
- Proprietary highly planarizing regrowth process with very low surface roughness

5. True GaN™ Devices

A p-n junction diode is one of the most basic two-terminal device that allows one to study the basic material properties. Analysis of diode performance allows one to study the basic quality of epitaxial layers using electrical metrics such as breakdown voltage and specific on-resistance.

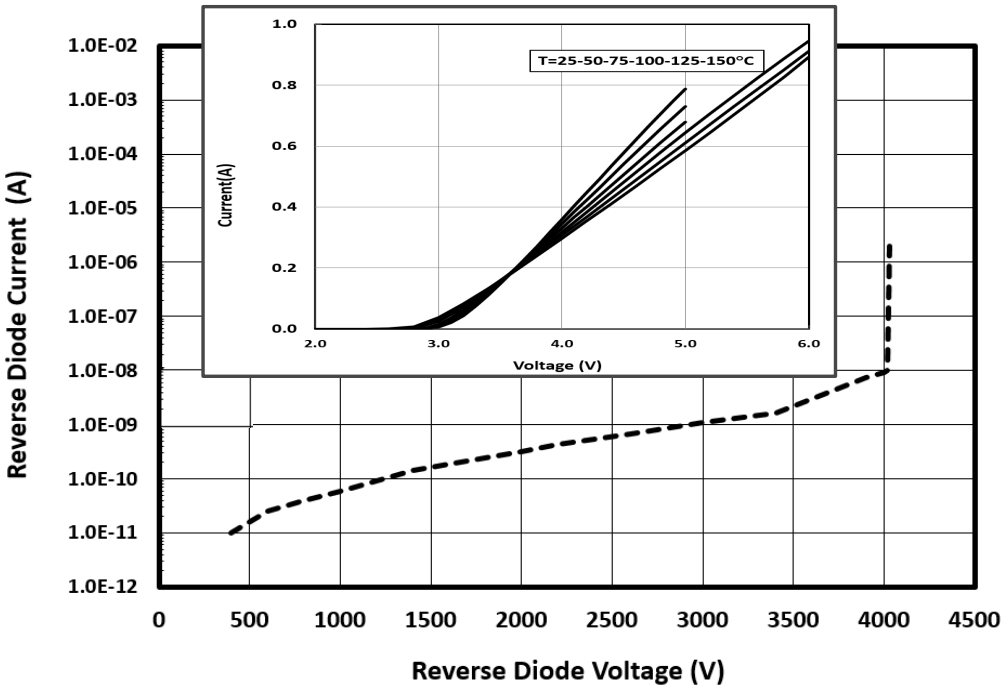


Figure 5: Diode characteristics with BV>4000V and $R_{on,sp}$=2.8mΩ.cm^2. Active die area was 0.12mm^2. Inset shows forward characteristics at different temperatures.

Using the True GaN™ technology described earlier, Avogy has successfully fabricated diodes with breakdown voltage >4000V and specific on-resistance 2.8mΩ.cm^2 (see Figure 5).

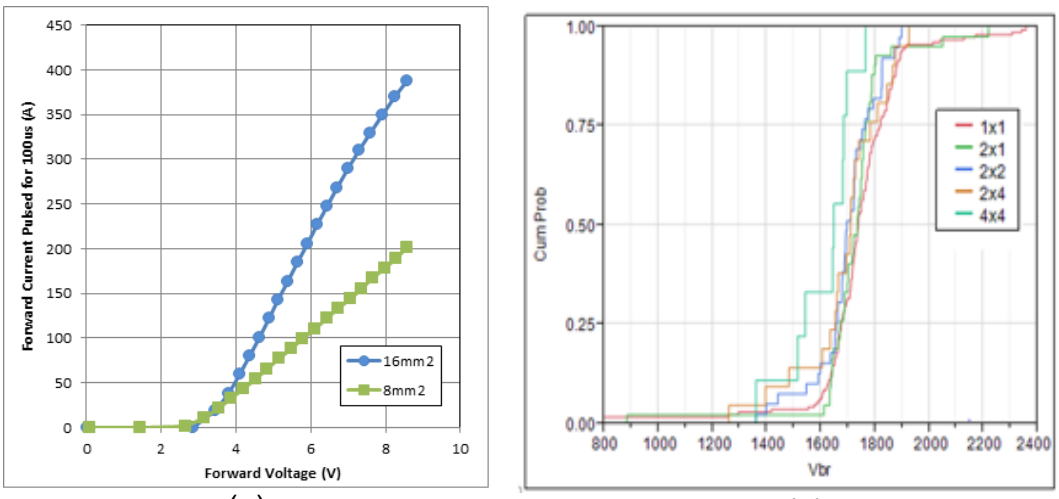


Figure 6: (a) Forward characteristics of high current diodes of 8mm^2 and 16mm^2 (b) Breakdown voltage distribution of diodes 1mm^2 to 16mm^2.

Avogy has also successfully created very high current (400A) diodes thereby scalability of the devices has also been demonstrated. Figure 6 shows the performance of these high current diodes.

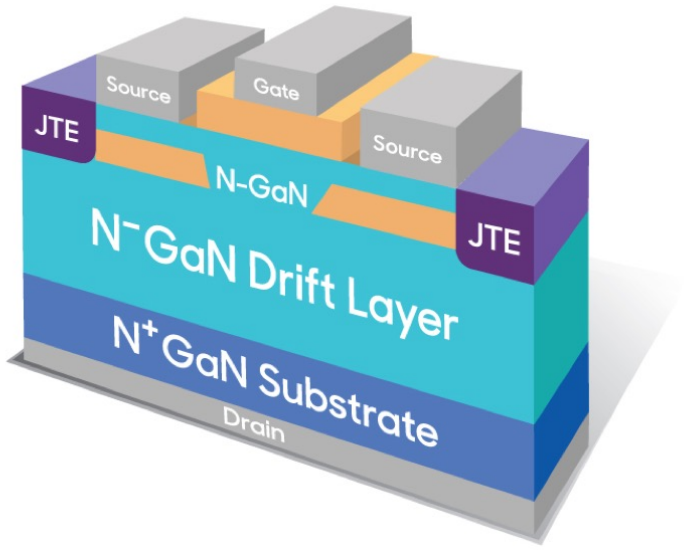


Figure 7: Artistic rendering of True GaN™ VJFET.

After having successfully demonstrated the True GaN™ technology for creating diodes, Avogy turned its focus on transistors. Diodes are the essential building blocks of junction field-effect transistors (JFET). Figure 7 shows an artistic rendering of True GaN™ vertical junction field-effect transistor (VJFET). Transistors are three terminal devices: Source terminal is the source of electrons, Drain terminal is the where the electrons wind up,

Gate terminal controls the conduction between Source and Drain by creating a potential barrier for electrons.

In ON-state, the Gate and Source terminals are grounded to zero potential and Drain potential is biased positively to a desired value. On-state resistance between the Drain and Source ($R_{DS,ON}$) determines the amount of current that flows between the Drain and the Source. In OFF-state, a negative bias is applied to the Gate which creates a potential barrier in the channel for electrons to travel from Source to Drain. Source remains grounded to zero potential and Drain potential can increase to values as high as the breakdown voltage. In OFF-state, the electric fields and thus leakage currents are highest. Junction Termination Extension (JTE) is used to terminate high electric fields at the edge of the device to realize the highest breakdown voltage.

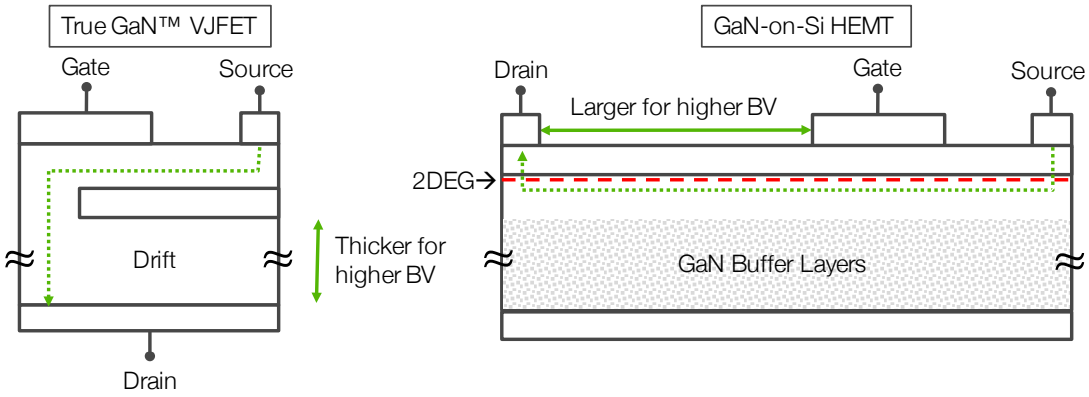


Figure 8: Schematic of True GaN™ VJFET and GaN-on-Si HEMT. Dotted green lines denote the electron conduction path between Source and Drain terminals. For higher breakdown voltage scaling in True GaN™ VJFET, Drift thickness is scaled up with no 2-D area penalty. In contrast, GaN-on-Si HEMT suffers an area penalty with Drain to Gate spacing.

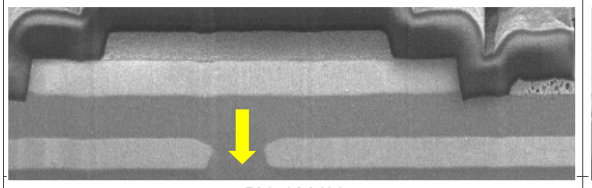
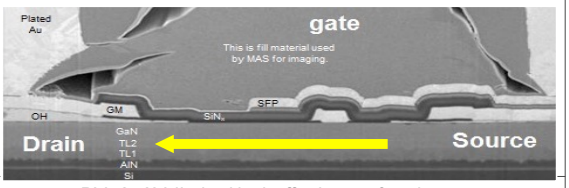
Figure 8 shows the schematics of True GaN™ VJFET and GaN-on-Si high electron mobility transistor (HEMT). In case of True GaN™, the substrate and the epitaxial layers are both GaN with extremely low defect densities. For higher breakdown voltage scaling in True GaN™ VJFET, drift thickness is scaled up with no 2-D area penalty. Avogy has demonstrated drift thickness of 40µm producing diodes with BV>4000V. In contrast, for GaN-on-Si HEMT Drain to Gate spacing needs to be increased for higher BV and thus it suffers an area penalty. But area penalty is not the only limitation for GaN-on-Si HEMTs. Leakage control between Drain and Source requires thicker epitaxial region. But the epitaxial region cannot be made too thick as it would increase the stress due to CTE mismatch between GaN and Si and lead to wafer warpage or breakage. GaN-on-Si is thus bounded by two limitations for higher breakdown voltages. It comes as no surprise that no GaN-on-Si HEMT is specified beyond BV=650V.

When reverse bias on a device exceeds the breakdown voltage, the electric field becomes high enough to cause free carriers to dislodge carriers from the lattice upon collision. These newly dislodged carriers create new carriers upon collision with lattice atoms. This "snow ball" effect causes a sudden increase in free carriers causing avalanche breakdown. True GaN™ VJFET has avalanche capability and thus allows reverse biased voltage to exceed the maximum BV value for a specified energy and current limitations. In GaN-on-Si HEMT, the leakage continues to gradually increase through sub-surface conduction and avalanche behavior is not realized.

GaN-on-Si HEMT rely on sheet of electron charge due to polarization (referred to as 2DEG) at the interface between AlGaN and GaN. This polarization charge is highly sensitive to traps at the AlGaN and nitride passivation interface. It is also affected by traps in the buffer layer below the channel. These traps can get charged and discharged due to gate bias and impacts the 2DEG to increase the resistance dynamically (or reduce the current—'current collapse').

A comparison between True GaN™ VJFET and GaN-on-Si HEMT is presented in Table 3. For same $R_{DS,ON}$, GaN die size is 4X smaller than GaN-on-Si HEMT at for BV=600V and 7X smaller for BV=1200V. Again, it should be pointed out that 1200V is purely fictional due to aforementioned limitations.

Table 3: Comparison of True GaN™ VJFET with GaN-on-Si HEMT

True GaN™ VJFET	GaN-on-Si HEMT
	
BV>1200V	BV<650V, limited by buffer layers & substrate
$R_{DS,ON}$ = 290mΩ 600V: 1.4 mm^2 (4X) 1200V: 1.7 mm^2 (7X)	$R_{DS,ON}$ = 290mΩ 600V: 6.0 mm^2 1200V (not possible): 12.0 mm^2
Avalanche capable	No avalanche capability
No dynamic $R_{DS,ON}$ (no current collapse)	Suffers from dynamic $R_{DS,ON}$ (current collapse)

Cost benefits of lower die size are obvious, but it also has additional benefits in reduction of input (C_{ISS}) and output (C_{OSS}) capacitances. Lower capacitances result in faster switching and lower input and output switching losses. Lastly, a key benefit of both True GaN™ and GaN-on-Si HEMT devices over Si based devices is that unlike Si-based devices, there is no body diode across the Drain and Source terminals. Thus, the reverse recovery charge (and thus time) is zero.

Baliga figure of merit (BFOM) for power semiconductor devices ($\epsilon_s \mu_n E_C^2$) relates the specific on-state resistance and breakdown voltage for a given material system. This relation is given by

$$R_{ON,SP} = \frac{4BV^2}{\epsilon_s \mu_n E_C^2} \quad (1)$$

Figure 9 shows the plot of breakdown voltage vs. specific on-state resistance for various devices. The lines denote the BFOM for the material system. The plot shows four different types of materials: True GaN™, GaN-on-Si, Si and SiC. Different manufacturers are designated by unique letters. We have shown only commercially available parts in this plot. Research accomplishments based on devices with impractical die sizes and manufacturing processes have not been considered.

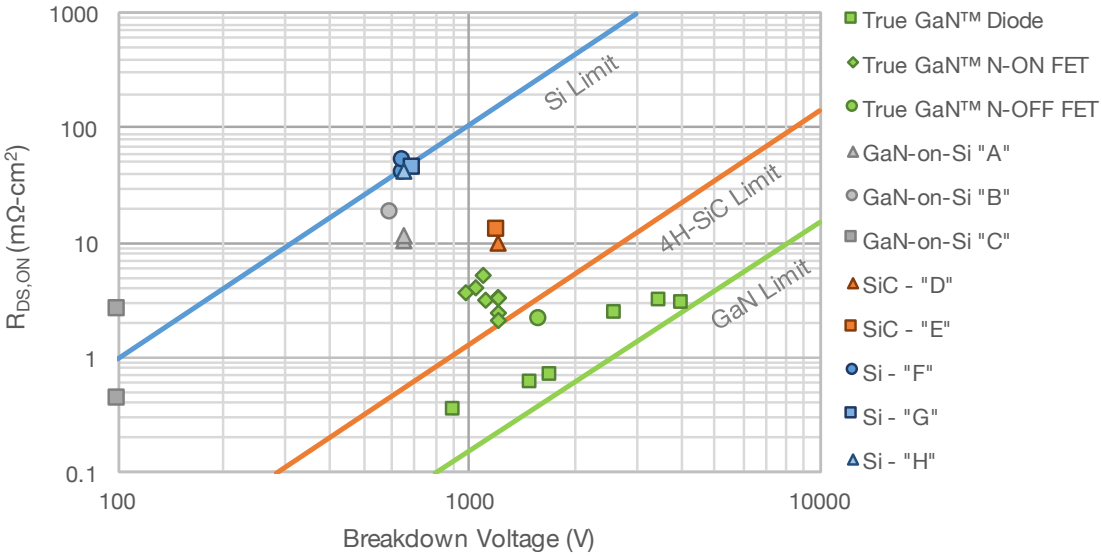


Figure 9: Performance comparison of True GaN™ VJFET vs. Si, SiC and GaN-on-Si devices from current manufacturers. No other material system currently matches the performance of Avogy's True GaN™ technology

Ideal region in the plot is for device to be in the lower right quadrant (low $R_{DS,ON}$ and high BV). It can be seen that no other material system currently matches the performance of Avogy's True GaN™ technology. Avogy continues to optimize its processes to achieve near-ideal performance for VJFET. Table 4 shows demonstration of $R_{DS,ON}$ scaling already achieved by Avogy.

Table 4: $R_{DS,ON}$ scaling of True GaN™ Normally-ON VJFET.

Production Year	BV_{DS} [V]	Die Size [mm^2]	$R_{DS,ON}$ [mΩ]
2016	900	1	660
	900	1.5	370
	900	2.25	210
	900	3.75	110
	900	6	72
2017	1200	1	850
	1200	1.5	483
	1200	2.25	273
	1200	3.75	153
	1200	6	91

Qualification of True GaN™ VJFET to be used in power systems requires reliability tests to pass stringent requirements. Avogy follows JEDEC specified stress conditions, and where applicable, supplemented with AEC.

6. Looking Ahead

Avogy is currently manufacturing a normally-ON or depletion-mode VJFET. Use of such devices requires a companion cascode device to create a normally-OFF operation. In order to eliminate the need for the cascoded configuration, feasibility of several normally-OFF architectures has been demonstrated. Normally-OFF transistor will be released to production in 2017.

There is a commonly held misconception about cost of die manufactured on bulk GaN wafers being too high due to expensive substrates. Currently, there are four major manufacturers, namely, Sumitomo (SEI), SCIOCS (ex-Hitachi), Mitsubishi Chemical (MCC) and Furukawa, that are ramping their production of 2” bulk GaN substrates to support LED, laser diode, and power electronics industries. As a result of increased demand and economies of scale, wafer costs have been reduced ~40% over that last 3 years. Additionally, each substrate manufacturer has plans 4” substrates. Many of them are already providing samples for evaluation. As demonstrated by the silicon industry, substrate costs will continue to come down with even higher volumes, competition and innovation in the future.

