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Characterization of vertical GaN p–n diodes and junction field-effect transistors on bulk GaN down to cryogenic temperatures

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Abstract

There is great interest in wide-bandgap semiconductor devices and most recently in vertical GaN structures for power electronic applications such as power supplies, solar inverters and motor drives. In this paper the temperature-dependent electrical behavior of vertical GaN p–n diodes and vertical junction field-effect transistors fabricated on bulk GaN substrates of low defect density \(10^4\) to \(10^6\) cm\(^{-2}\) is described. Homoeptaxial MOCVD growth of GaN on its native substrate and the ability to control the doping in the drift layers in GaN have allowed the realization of vertical device architectures with drift layer thicknesses of 6 to 40 \(\mu\)m and net carrier electron concentrations as low as \(1 \times 10^{15}\) cm\(^{-3}\). This parameter range is suitable for applications requiring breakdown voltages of 1.2 kV to 5 kV. Mg, which is used as a p-type dopant in GaN, is a relatively deep acceptor \(E_A \approx 0.18\) eV) and susceptible to freeze-out at temperatures below 200 K. The loss of holes in p-GaN has a deleterious effect on p–n junction behavior, p-GaN contacts and channel control in junction field-effect transistors at temperatures below 200 K. Impact ionization-based avalanche breakdown \((BV > 1200\) V\) in GaN p–n junctions is characterized between 77 K and 423 K for the first time. At higher temperatures the p–n junction breakdown voltage improves due to increased phonon scattering. A positive temperature coefficient in the breakdown voltage is demonstrated down to 77 K; however, the device breakdown characteristics are not as abrupt at temperatures below 200 K. On the other hand, contact resistance to p-GaN is reduced dramatically above room temperature, improving the overall device performance in GaN p–n diodes in all cases except where the n-type drift region resistance dominates the total forward resistance. In this case, the electron mobility can be deconvolved and is found to decrease with \(T^{-3/2}\), consistent with a phonon scattering model. Also, normally-on vertical junction field-effect transistors with \(BV = 1000\) V and drain currents of 4 A are fabricated and characterized over the same temperature range. It is demonstrated that vertical GaN devices (diodes and transistors) utilizing p–n junctions are suitable for most practical applications including automotive ones \((210\) K < \(T < 423\) K). While devices are functional at cryogenic temperatures \((77\) K) there may be some limitations to their performance due the freeze-out of Mg acceptors.

Keywords: GaN vertical transistor, GaN cryogenics, GaN power diode

(Some figures may appear in colour only in the online journal)

1. Introduction

Power electronics is the interface between an electrical source and a load. The source and load can differ in frequency, amplitude and the number of phases. In a power electronic system electrical power flow, voltages and currents are converted from one form to another. Examples include a laptop charger converting 110–260 V ac power to 19 V dc power, a
solar inverter converting 48 V dc power to 220 V ac power, an electrical vehicle (EV) drive using 200 V dc battery power to drive a 650 V ac motor, and a three-phase motor driver in a hybrid vehicle [1]. The building blocks comprising a power electronics system are power semiconductor devices, gate drivers and controller circuits. It is expected that power electronic systems are operational in a large range of environmental conditions. For example the temperature range of power electronics for automotive applications can be from $-60^\circ\text{C}$ to $150^\circ\text{C}$ ($213\text{ K}$ to $423\text{ K}$). The needs of the power semiconductor components of power electronic systems have been well addressed by silicon-based diodes ($\text{Si}$ diodes, $\text{p-i-n}$ diodes) and transistors (metal–oxide–semiconductor field-effect transistor (MOSFET) and insulated gate bipolar transistor (IGBT)). An impressive reduction in size and improvements in efficiency, weight and power density of systems have resulted from the advancing performance of silicon-based power semiconductor devices. However, the performance of devices based on silicon is at the fundamental material limits of silicon. This limitation has resulted in a rapid expansion of efforts to develop wide-bandgap power semiconductor alternatives because further reductions in size and weight, and an increase in efficiency in power electronic systems, can be achieved by utilizing SiC [2] and GaN [3–6].

There are many reasons for developing GaN-based power devices. First, the fundamental (material-based) figure-of-merit parameters for GaN are better than for SiC and significantly better than for Si. Specifically, some of the desirable properties associated with GaN and its related alloys and heterostructures include high bandgap energy ($E_{\text{C}} \approx 3.4\text{ eV}$) and hence low intrinsic carrier concentration (useful for high-temperature operation), favorable transport properties (large electron mobility and saturation velocity), a high critical breakdown electric field and high thermal conductivity [7–11]. Second, the emergence of the GaN-based solid-state lighting [12–14] and radio-frequency (RF) electronics [15] industries has paved the way in fundamental understanding of substrate technology, epitaxial growth using MOCVD (metalorganic chemical vapor deposition) processes, fabrication methods (etching, metallization), packaging (die attach, substrate thinning), testing and reliability [16–18].

For power electronics the figure of merit of a power semiconductor device captures the trade-off between two modes of operation. In the conduction mode it is desired that the device exhibit a low resistance as described by its specific resistance ($R_{\text{sp}}$), while in the blocking mode the device supports a large breakdown voltage (BV). These conflicting requirements (for a unipolar power device) have been captured and formulated [19] as $\text{BV}^2/R_{\text{sp}} \sim \mu_0 E_{\text{C}}^3$, where $\mu_0$ is the mobility of electrons and $E_{\text{C}}$ is the critical electric field at which breakdown occurs. The advantage of wide-bandgap semiconductor devices over silicon devices arises from the cubic dependence of the figure of merit on the critical electric field. While the critical electric field for silicon is 0.3 MV cm$^{-1}$ we estimate a value of at least 3.5 MV cm$^{-1}$ for bulk GaN and possibly as high as 3.75 MV cm$^{-1}$. A detailed discussion is given in [19–22]. This value for the critical electric field and an electron mobility of 900–1800 cm$^2$ V$^{-1}$ s$^{-1}$ forms the basis of the ‘theoretical limits’ for GaN. It is acknowledged that the concept of a critical electric field in the context of non-stationary transport and in light of the complicated non-isotropic band structure of GaN [23–25] is overly simplistic. We choose to use it here since the power semiconductor literature has adopted its use for benchmarking purposes. Table 1 summarizes the material parameters for semiconductor materials that are practical and currently suitable for power applications, namely Si, SiC and GaN.

Figure 1. Schematic of the GaN vertical $\text{p-n}$ diode and junction field-effect transistor on bulk GaN.
Table 1. Fundamental material parameters for Si, SiC and GaN [8–10, 20–22].

<table>
<thead>
<tr>
<th>Material</th>
<th>(\mu_n) (cm(^2) V(^{-1}) s(^{-1}))</th>
<th>(E_C) (MV cm(^{-1}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1350</td>
<td>0.25</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>720</td>
<td>2.0–3.0</td>
</tr>
<tr>
<td>GaN</td>
<td>900–1800</td>
<td>3.2–3.75</td>
</tr>
</tbody>
</table>

GaN-based Schottky diodes have already been commercialized and are commonly utilized in applications that demand higher efficiency. However, the performance and reliability of lateral GaN-based devices has fallen short of their potential. This is because GaN layers grown on mismatched foreign substrates (e.g. Si or SiC) create difficulties for realizing vertical device structures and have higher defect densities (>10\(^8\) to 10\(^9\) cm\(^{-2}\)). Low defect density is important in power devices because it can affect the performance characteristics (e.g. breakdown voltage and off-state leakage current), yield and reliability (high-temperature reverse bias and operating life, avalanche ruggedness). For GaN/InGaN lasers significant improvements in performance and reliability have been demonstrated using bulk GaN substrates of low defect density [12, 14]. It is generally recognized that lateral device architectures (high electron mobility transistors) are less well suited to power applications, while vertical structures are optimal for achieving devices with higher breakdown voltage and current without paralleling (monolithic), suffer less from thermal management issues associated with thin film surfaces and yield more die on a wafer. It should be noted that all high-voltage (BV > 600 V) Si- or SiC-based devices are vertical architectures. Furthermore, vertical structures fabricated on bulk GaN substrates are expected to be more reliable due to the lack of mismatched interfaces and insensitivity to surfaces. The reason that there have been so few reports of vertical GaN power devices has been the lack of availability of bulk GaN substrates with low defect density (<10\(^8\) cm\(^{-2}\)). A related reason is the assumption that bulk GaN substrates are too expensive to be commercially viable. However, currently there are already multiple suppliers of bulk GaN substrates. The material quality has been improving rapidly due to research and development [26–28] and the demand and scale of the optoelectronics industry are driving the prices down.

In this paper the temperature-dependent electrical behavior of state-of-the-art vertical GaN p–n diodes and vertical junction field-effect transistors fabricated on bulk GaN substrates of low defect density (10\(^4\) to 10\(^6\) cm\(^{-2}\)) is described. In the case of the p–n diodes special attention is given to their avalanche breakdown characteristics caused by impact ionization. Impact ionization-based avalanche breakdown in GaN p–n junctions is characterized between 77 K and 423 K for the first time. The electrical parameters of interest for the vertical junction field-effect transistor are the transfer characteristics (threshold voltage), output characteristics (source–drain resistance and saturation drain current) and turn-off (leakage current) behavior.

2. Device fabrication and processing

The device structures are shown in figure 1. The structure on the left is a p–i–n diode while that on the right is a vertical junction field-effect transistor. In both devices there are three regions of interest. Firstly, the core of the device; in the case of the diode this is the p–n junction, for the transistor it is the device channel, gate regions and the aperture. Secondly, the lightly doped drift region, and thirdly, the edge termination/isolation region, which are common to both device types.

In this study the device structures are designed for a breakdown voltage of 1200 V. The maximum breakdown voltage of the device is determined by the design of the n-type doping of the drift layer and its thickness, along with the edge termination scheme. The nominal net doping density of the drift region for the devices in this study is \(N_D - N_A = 1 \times 10^{16} \text{ cm}^{-3}\), while the drift layer thickness is 15 \(\mu\)m. The net doping (\(N_D - N_A\)) also determines the conductivity in forward direction when the devices are conducting, and the depletion depth in reverse bias. Consequently, for kV-level operation net doping control in the n-type drift layer in the range 10\(^{15}\)–10\(^{16}\) cm\(^{-3}\) is crucial. An edge termination structure spreads the potential applied to the top metals over a distance that is typically greater than the thickness of the drift region. The process uses two separate implant steps. This technique of smoothing the equipotential contours at the edges of the devices results in a manageable surface electric field and prevents the device from breaking down prematurely [29, 30]. In the p–n diode process, 0.5 \(\mu\)m p-type layers are doped with Mg, at 2 \(\times\) 10\(^{19}\) cm\(^{-3}\), and a higher-doped layer at the surface for reduced contact resistance. P-type material has been characterized by Hall measurements, which indicate a room-temperature hole concentration of 4 \(\times\) 10\(^{17}\) cm\(^{-3}\) and a mobility of 12 cm\(^2\) V\(^{-1}\) s\(^{-1}\). In the transistor process narrow trenches are etched using a Cl-based chemistry in an inductively coupled plasma (ICP) process. An n-type GaN layer is regrown to fill the trenches and form a channel above the patterned p-type GaN layer (buried gate). Finally, the p-type GaN layer was deposited and patterned to form the top gate. The thickness and doping of the n-GaN layer in the channel region were designed to target the threshold voltage of about \(V_{th} = -20\) V. The length of the channel region was chosen to be sufficient to preclude the effect of the drain voltage on the potential barrier in the channel in the off-state. The SEM cross section of the transistor is shown in figure 2 (top). The buried p-body layer can be contacted using an appropriate metal for ohmic contact to p-type GaN, such as Pd, Pt or Sc. In these devices, a Pd-based stack was utilized. Since it is very difficult to achieve good ohmic contacts to ICP-etched p-GaN surfaces a p-GaN plug process is used as shown in figure 3 (bottom). The source electrode is Ti/Al-based. A SiN\(_x\)-based film serves as an interlayer dielectric (ILD) that is deposited by plasma-enhanced chemical vapor deposition (PECVD). Via contact holes were patterned for both the source and the gate. Finally, 4 \(\mu\)m thick source and gate pad metals were deposited for wire bonding and current spreading. A backside contact (drain) was formed by evaporating proprietary metallization onto the bottom of an n\(^+\)-type GaN substrate.
after the substrate was lapped, polished and ICP-etched down to 6 mils (0.15 mm). The backside process is common to both diodes and transistors. As mentioned above, Mg, which is used as a p-type dopant in GaN, is a relatively deep acceptor ($E_A \approx 0.18$ eV) and susceptible to freeze-out at temperatures below 200 K [31]. The loss of holes in p-GaN can have a deleterious effect on p–n junction behavior, p-GaN contacts and channel control in junction field-effect transistors at lower temperatures.

Figure 3(a) shows the calculated change in hole concentration (Mg doping) and electron concentration (Si doping) in GaN with temperature. While both electron and hole concentrations drop as temperature is reduced, the effect is much more profound for holes, especially below 200 K. Reduction in the concentration of holes reduces the conductivity in the p-regions and interferes with our ability to form low-resistance ohmic contacts as shown in figure 3(b). On the other hand at higher temperatures (e.g. 423 K) the contact resistance to p-GaN improves significantly and contributes to the improved performance of GaN p–n diodes at elevated temperatures. For the junction field-effect transistor, the p-GaN regions are used as gate material to control the potential in the channel and the current flow from source to drain. The impact of Mg freeze-out is less severe during steady-state transistor operation but will have an impact during transients and hamper the switching behavior of the transistor.

3. Electrical results on GaN p–n diodes

$I$–$V$ and $C$–$V$ measurements from 79 K (−194 °C) to 423 K (150 °C) were performed on GaN p–n diodes housed in TO-220 power packages. The active die area (anode metal) is 0.72 mm². Figure 4 shows the diode forward current on a linear (a) and a logarithmic (b) scale. As expected, the p–n diode turns on at 3 V at room temperature, and with decreasing temperature the turn-on voltage increases. The GaN p–n diode is functional at 80 K but suffers from a lack of holes available for recombination or injection as the forward bias is increased.

As the diode temperature is increased from room temperature to 423 K (150 °C) two competing factors play out. The contribution to resistance from the p-GaN and p-GaN ohmic contact decreases while the resistivity of the drift region increases. Hence, the overall p–n diode performance is not sensitive to increasing temperature. This behavior has been discussed before in [22] in detail. These diodes are capable of delivering 10–20 A of current at room temperature as the forward voltage is increased [21, 22, 32].
In figure 5(a) the I–V characteristics of a reverse-biased GaN p–n diode are given between 80 K and 415 K. It can be seen that the reverse leakage current of the diode improves (is reduced) by lowering the ambient temperature. This behavior is typical of leakage current generated from recombination centers in the depletion region. At higher voltages the diode goes into avalanche breakdown that comes about from impact ionization. The current was limited to 5 μA during this test. The breakdown voltage is plotted versus temperature in figure 5(b). It should be noted that while the leakage current due to recombination increases with temperature, the device breakdown voltage also increases with temperature. This result is achieved because the p–n junctions are fabricated on high-quality (lower defect density) GaN substrates. The device breakdown voltage is about 1400 V at room temperature. At temperatures below about 200 K the breakdown behavior is not as abrupt and a soft breakdown is observed. We attribute this to the Mg freeze-out effect.

For power switching and rectifying applications, the ruggedness in breakdown is a critical requirement as supplementary snubber circuits impose a performance and efficiency penalty on the system. Inductive avalanche capability and ruggedness characterization of vertical GaN p–n junction diodes grown on native GaN substrates demonstrate that diodes based on the technology described here can sustain reverse currents as high as 10 A (for area = 0.36 mm² and 2.8 kA cm⁻²) in breakdown [33]. The work presented here is the first demonstration of breakdown voltage in GaN p–n junctions down to cryogenic temperatures.

4. Electrical characterization of vertical junction field-effect transistors

GaN normally-ON vertical junction field-effect transistors used in the temperature study are housed in PQFN packages.
The PQFN packaged devices were soldered to small printed circuit boards with pins designed for standard TO-220 sockets. For measurements below room temperature, the devices were placed in a liquid nitrogen-cooled temperature control system. This system provides for temperature measurement of the device by means of a thermocouple pressed onto the top side of the PQFN package. For measurements above room temperature, the devices were placed into a precision temperature-controlled chamber with a heated dry nitrogen stream maintaining the temperature of the device at the set-point. The maximum temperature in the measurements was limited to 423 K (150 °C) due to the temperature limitation of the PQFN package. In all measurements, the temperature control accuracy was limited to ±15°C due to measurement-induced errors and temperature variations caused by self-heating. Figure 6 shows the output characteristics of a representative device at various temperatures. The transistor is operational between 123 K (−150 °C) and 423 K (150 °C). However, there is inadequate gate control at liquid nitrogen temperature as indicated by the leakage at $V_G = −30$ V and the strong self-heating effects observed in the saturation region. Figure 7(a) depicts the temperature-dependent threshold voltage extracted from $(I_D - V_G)$ measurements at a drain bias of 5 V. The inadequate gate control seen in figure 6(d) is then attributed to the strong temperature dependence of the threshold voltage below −100 °C and the shifting of the threshold voltage to less than −30 V at 77 K (−196 °C).

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Figure 6. Output characteristics of the packaged devices at (a) 123 K (−150 °C), (b) 300 K (27 °C), (c) 423 K (150 °C), (d) 77 K (−196 °C). The measurements were performed using 300 μs voltage pulses. The gate bias was stepped at the following voltage values: −30, −20, −17.5, −15, −12.5, −10, −7.5, −5, −2.5, 0 V.
phonon scattering-dominated mobility. Similarly, the reduction in $I_{DS}$ is much faster than the reduction dictated by saturation velocity with increasing temperature. The device active area is about 0.4 mm$^2$, which translates to a current density of 1.0 kA cm$^{-2}$ and device specific resistivity of about 5 m$\Omega$ cm$^2$ at room temperature.

The temperature-dependent leakage data shown in figure 8 show that the devices can be considered to be functional between 123 K ($-150 \degree C$) and 423 K ($+150 \degree C$). However, at 77 K ($-196 \degree C$) the device cannot sustain high drain biases even when the gate bias is reduced to $V_G = -40 \, V$. The $V_G = -40 \, V$ leakage data presented in figure 8 indicate that the issue with the transistor operation below 123 K ($-150 \degree C$) is related to the strong reduction in the breakdown voltage of the p–n junction diode observed at similarly low temperatures. Figure 8 also demonstrates that at temperatures below room temperature the breakdown voltage exhibits a negative temperature coefficient and the reverse leakage characteristic has a soft breakdown. On the basis of these features, it is considered that at reduced temperatures, the voltage blocking capability is limited by defect-induced leakage. At room temperature and above, the breakdown voltage has a positive temperature coefficient and the breakdown is sharp, suggesting that the breakdown may be brought on by impact ionization-based avalanche multiplication, although much work has to be performed to confirm this. The strong increase in leakage at high temperatures seen in figure 8 is another factor that may limit the operational range of the device. From Arrhenius analysis of the 900 V leakage data we infer that the leakage current is dominated by defects and we extract an activation energy of about 1 eV.

5. Conclusions

There is great interest in wide-bandgap semiconductor devices and most recently in vertical GaN structures for power electronic applications. In this paper the temperature-dependent electrical behavior of vertical GaN p–n diodes and vertical junction field-effect transistors fabricated on bulk GaN substrates of low defect density ($10^4$ to $10^6$ cm$^{-2}$) is described down to cryogenic temperatures. Mg, which is used as a p-type dopant in GaN, is a relatively deep acceptor ($E_A \approx 0.18$ eV) and susceptible to freeze-out at temperatures below 200 K. The loss of holes in p-GaN has a deleterious effect on p–n junction behavior, p-GaN contacts and channel control in junction field-effect transistors at temperatures below 200 K. Impact ionization-based avalanche breakdown (BV $> 1200 \, V$) in GaN p–n junctions is characterized between 77 K and 423 K for the first time. At higher temperatures the p–n junction breakdown voltage improves due to increased phonon scattering. A positive temperature coefficient in the breakdown voltage is demonstrated down to 77 K; however, the device breakdown characteristics are not as abrupt at temperatures below 200 K. Normally-on vertical junction field-effect transistors with BV $= 1000 \, V$ and drain currents of 4 A are characterized over the same temperature range. It is demonstrated that vertical GaN devices (diodes and transistors) utilizing p–n junctions are suitable for most practical applications including automotive ones ($210 \, K < T < 423 \, K$). While devices are functional at cryogenic temperatures (77 K) there may be some limitations to their performance due the freeze-out of Mg acceptors.
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References


