Late News Paper

Vertical Power Diodes in Bulk GaN

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***Abstract*—Vertical diodes with breakdown voltages up to 2.6kV have been fabricated on bulk GaN substrates. The measured figures-of-merit of these devices show performance near the theoretical limit of GaN. These vertical GaN diodes exhibit robust avalanche breakdown behavior with a positive temperature coefficient. System-level performance advantages have been demonstrated in power conversion applications. Statistical data have been collected from thousands of devices. Initial reliability tests have been completed.**

I. INTRODUCTION

Most power electronics experts agree that silicon power devices are approaching the physical limits of silicon. As such, there is a growing effort in the development of alternative materials, such as silicon carbide (SiC) and gallium nitride (GaN), to enable the continued improvement of the size and efficiency of power electronics. SiC diodes have already been commercialized and are increasing market share in applications that demand the highest efficiency. There is great interest in developing GaN-based power devices because the fundamental material based figure-of-merit (FOM) of GaN is at least 5X better than SiC and nearly 1000X better than Si. To date, almost all of the GaN power device development effort has been directed toward lateral devices, such as high-electron mobility transistors (HEMTs), fabricated in thin layers of GaN that are grown on foreign substrates. However, the performance and reliability of these lateral GaN devices have fallen well short of expectations. By fabricating vertical power devices on bulk GaN substrates, it is possible to realize the true potential of GaN.

II. VERTICAL VS. LATERAL GAN DEVICES

Lateral GaN power devices suffer from several shortcomings that have limited their technical and commercial success to date. GaN layers grown on foreign substrates (e.g. sapphire, silicon, or silicon carbide) have a high defect density ($> 10^8$ cm^{-2}). In contrast, vertical GaN devices are fabricated in homoepitaxial GaN layers grown on low defect density bulk GaN substrates. Using a native substrate provides more than a 1000X improvement in defect density ($< 10^5$ cm^{-2}). Expert opinions vary on the impact of these defects on device performance and reliability, but most agree that it is preferable to make devices in a material that has fewer defects.

Lateral GaN power device technologies typically include buffer layers that separate the thin GaN drift region from the foreign substrate. These buffer layers are prone to charge trapping effects that cause problems with device performance and reliability. In addition, the buffer layers are generally poor thermal conductors, limiting the thermal performance of lateral GaN power devices. Moreover, the buffer layers are highly stressed, causing wafer bowing that limits the maximum thickness of these layers. Thus, the maximum blocking voltage achievable in lateral GaN devices is generally considered to be less than 1200V. Growing homoepitaxial GaN on bulk GaN substrates does not require any buffer layers. Therefore, there are no charge trapping effects and no barriers to heat removal. Furthermore, very thick epitaxial layers are possible, allowing the fabrication of vertical power devices with very high breakdown voltage (BV).

Lateral GaN devices have additional problems associated with their lateral current flow near the buffer layers and overlying dielectric layers. These well-known issues include current-collapse, dynamic on-resistance, and inability to support avalanche breakdown. In vertical GaN devices, on-state current flows down through the homoepitaxial layer in the interior portion of the device. As such, these devices are immune from current collapse and dynamic on-resistance. Moreover, our vertical GaN devices exhibit true avalanche breakdown and can withstand high avalanche energies.

The fundamental benefits of GaN, coupled with the many shortcomings of existing lateral GaN structures, provide ample motivation to develop vertical power devices in bulk GaN substrates. This paper reports progress on the first significant effort to commercialize such devices.

III. DEVICE FABRICATION

Fig. 1 shows schematic cross-section drawings of our vertical GaN Schottky Barrier Diodes (SBDs) and PN Diodes. These diodes were fabricated on 2-inch bulk GaN substrates with N^{++} doping. Homoepitaxial layers were grown by metal-organic chemical vapor deposition (MOCVD). Depending on the desired BV, the N-type drift-layer layer doping was in the range of 1 to $3x10^{16}$ cm^{-3} and thicknesses were in the range of 5 to 20 μm. SBDs were fabricated by the deposition and patterning of palladium on the GaN epitaxial layer. PN diodes were fabricated by in-situ growth of a magnesium-doped P^+ GaN epitaxial layer on top of the N-type GaN epitaxial drift region, followed by deposition and

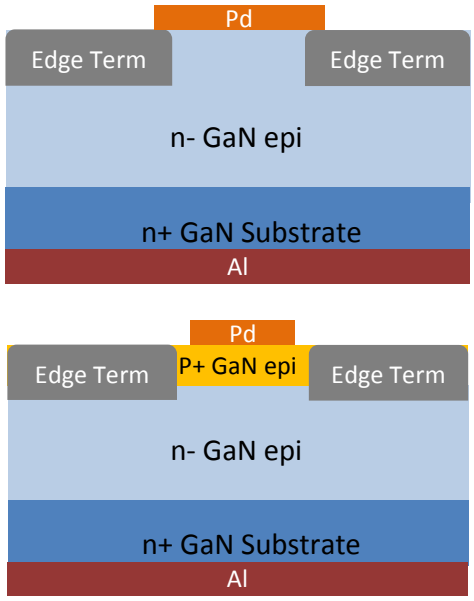

Figure 1. Schematic cross-sections of SBDs and PN diodes

patterning of palladium to contact the P-type GaN. The P^+ GaN layer had a hole concentration of about $5x10^{17}$ cm^{-3} and a hole mobility of about 11 cm^2/V-sec at 25°C as measured by Hall Effect. A proprietary edge termination structure was employed to terminate the devices and realize BVs approaching 85% of theoretical parallel-plane junction breakdown. Backside contacts were formed by evaporating aluminum onto the back surface of the N-type GaN substrate.

IV. Device Characterization

Fig. 2 shows pulsed forward current-voltage measurements of SBD and PN diodes with different epi layers designed for 600V and 1200V minimum BV, respectively. The SBD exhibits a forward knee voltage of about 0.9V, as expected from the work function of palladium and the bandgap of GaN. The PN diode has a knee voltage of about 3.0V, as expected for GaN. These devices have active areas of less than

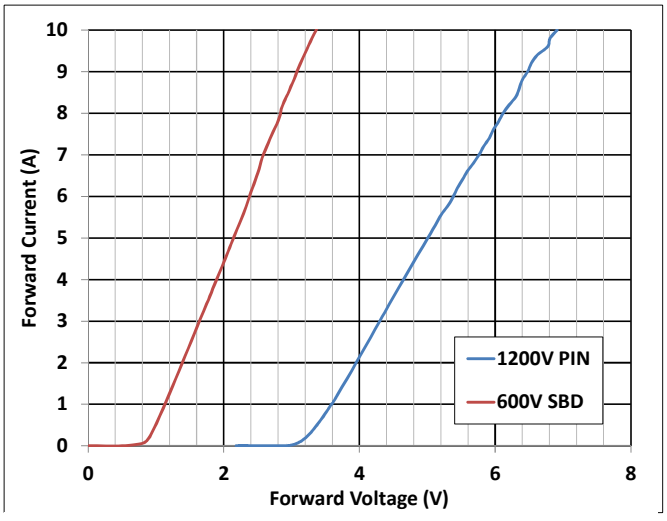

Figure 2. Pulsed forward I-V characteristics of SBDs and PN diodes

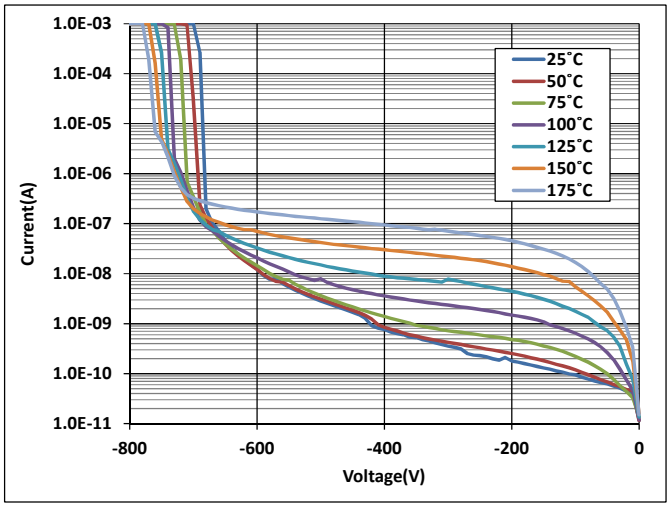

Figure 3. Reverse I-V characteristics of PN diodes as a function of temperature.

$0.5mm^2$, yet are capable of handling pulsed currents (300µs pulse width) in excess of 10A.

Fig. 3 shows the off-state characteristics of a PN diode designed for 600V minimum BV. Reverse current vs. voltage data are shown for device temperatures of 25˚C to 175˚C in 25˚C increments. The leakage current increases exponentially with temperature, but remains reasonably low all the way to breakdown. The breakdown voltage exhibits a positive temperature coefficient, indicative of avalanche breakdown.

Fig. 4 demonstrates the avalanche energy capability of our vertical GaN PN diodes, showing the reverse current versus reverse voltage characteristics of several devices designed for 1700V minimum BV. These devices were driven into avalanche breakdown using current pulses, with a pulse width of 30ms, up to 15mA and 2000V, representing an energy capability of more than 900mJ. This characteristic is in sharp contrast to previously-reported lateral GaN devices, which have essentially no avalanche capability.

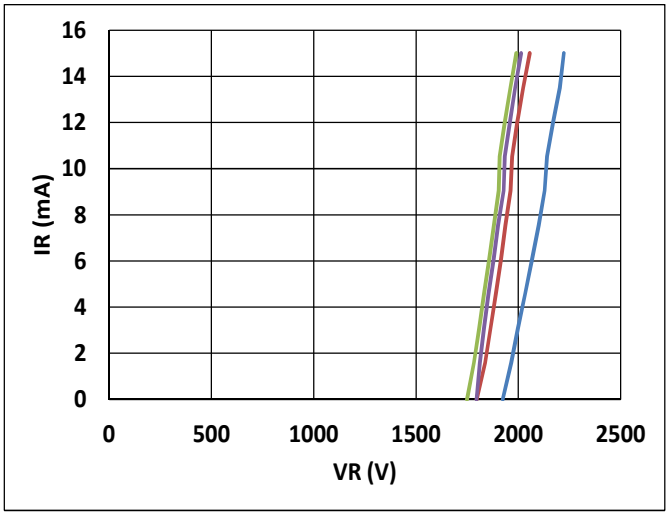

Figure 4. Pulsed reverse I-V characteristics of PN Diodes

Fig. 5 shows a graph of the well-known power device figure-of-merit (FOM), showing how the on-state and off-state performance are governed by the physical properties of the semiconductor material. On-state performance is represented by specific on-resistance (Rsp), which is on-resistance multiplied by the active surface area required to achieved that on-resistance. Off-state performance is represented by breakdown voltage (BV), which is the maximum voltage a power device can block when it is reverse biased. The fundamental limits for the drift region resistance of unipolar devices fabricated in SiC and GaN are shown by solid lines. Published results from vertical SiC power devices plotted in this figure show that commercial SiC devices are already approaching the theoretical limit for this material system [1-4]. Published results from lateral GaN power devices fabricated on sapphire, SiC, or silicon substrates are also included in Fig. 5. It is clear that the performance of these devices is far from the fundamental GaN limit. In fact, almost none of the reported lateral GaN devices have even surpassed the performance of SiC devices [5-7].

There have been very few publications of vertical GaN power devices, but these early results, shown as black squares in Fig. 5, verify the potential of GaN to exceed the performance of SiC and lateral GaN devices [8-10]. Measured results from our fabricated vertical GaN diodes are shown by the green data points in Fig. 5. The dashed green line represents simulated ideal performance when the substrate resistance is added to the drift region resistance indicated by the solid green FOM line. Our devices exhibit BVs of 900V – 2600V with FOM well below the SiC limit and very close to the theoretical limit of GaN.

V. Applications Evaluation

We designed a 300 kHz, 20W off-line LED driver to demonstrate the performance advantages of our 600V vertical GaN SBD. Fig. 6 shows the measured efficiency of this LED driver as a function of output power, showing how the overall system performance is affected by the type of boost diode used in the circuit. The GaN diode provides a significant

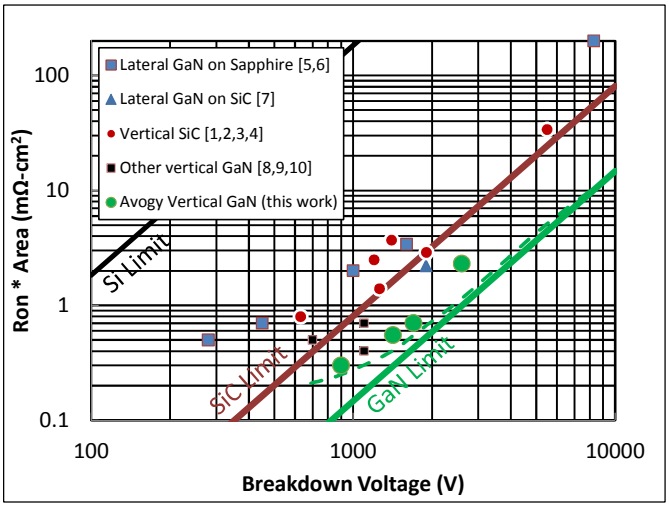

Figure 5. Power device FOM plot comparing Avogy vertical GaN diodes with other SiC, lateral GaN, and vertical GaN devices

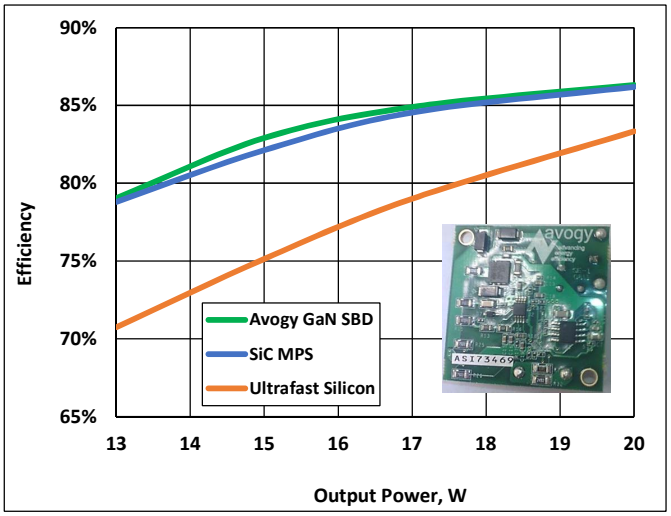

Figure 6. Efficiency comparison of vertical GaN, SiC, and Si diodes in an off-line LED driver circuit

improvement in system efficiency compared to a similarly-rated ultrafast silicon diode, and a slight performance improvement over a SiC merged PN-Schottky (MPS) diode. The inset of Fig. 6 shows a picture of the LED driver demonstration board.

VI. Yield and Reliability

The vertical diodes reported in this paper were fabricated on 2-inch bulk GaN substrates. Fig. 7 is a photograph of a completed wafer containing nearly 1000 devices. We have processed dozens of these wafers and tested several thousand devices. Process and design optimization have resulted in yields that are impressively high for a new material system, and well above the yields reported for lateral GaN devices fabricated on SiC or Si substrates.

Initial reliability testing has been completed on 1200V GaN diodes assembled in industry-standard TO-220 packages. A full suite of tests including high-temperature reverse bias (HTRB), high-temperature operating life (HTOL),

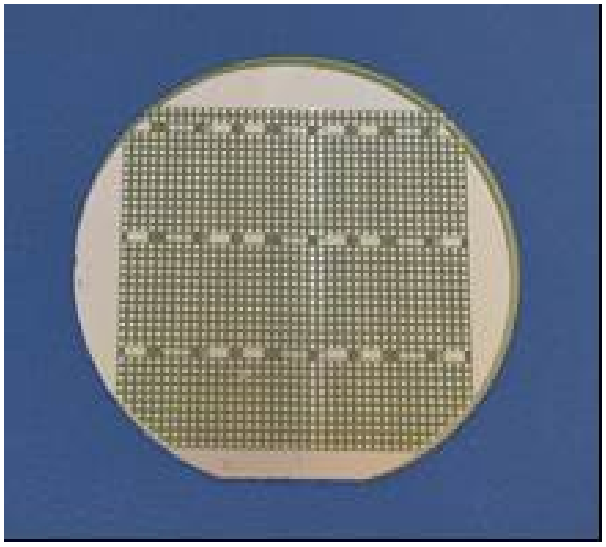

Figure 7. A 2-inch bulk GaN wafer with fabricated diodes

temperature humidity bias (THB), temperature cycling (TC), and high-temperature storage (HTS) were performed for at least 1000 hours. Of the hundreds of parts subjected to these tests, only a few failures were found, and none that related to fundamental material properties.

CONCLUSIONS

We have fabricated vertical SBD and PN diodes with breakdown voltages up to 2600V on bulk GaN wafers. These devices exhibit high current densities, avalanche breakdown, and low leakage. The demonstrated power device figures of merit are far better than previously reported results for SiC devices and lateral GaN devices, approaching the fundamental limits of GaN. Our diodes have been operated in power supply applications and compared with Si and SiC devices, demonstrating system-level performance advantages. Commercial viability has been established by yield optimization and preliminary reliability testing.

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